0907432 Computer Design (Spring 2010) <u>Quiz 1A</u>

رقم التسجيل: رقم الشعبة:

<u>Instructions</u>: Time **15** minutes. Closed books and notes. No calculators. Please answer all problems in the space provided. **No questions are allowed**.

<Good Luck>

Q1. Consider the following data:

Processor	Clock rate	No. instructions	Time
P1	2.0 GHz	20 x 10 ⁹	7 s
P2	1.5 GHz	30 x 10 ⁹	10 s

Find the clock rate for P2 that reduces its execution time to that of P1.

 $Time_{new}/Time_{old} = 7/10 = 0.7$

So $f_{\text{new}} = f_{\text{old}}/0.7 = 1.5 \text{ GHz}/0.7 = 2.14 \text{ GHz}.$

Q2. Find all data dependencies in the following instruction sequence. For every data dependence, identify its type, the instructions involved, and the dependence location.

I1: lw \$1,40(\$2)

I2: add \$2,\$3,\$3

I3: add \$1,\$1,\$2

I4: sw \$1,20(\$2)

RAW:

(\$1) I1 to I3

(\$2) I2 to I3, I4

(\$1) I3 to I4

WAR:

(\$2) I1 to I2

WAW:

(\$1) I1 to I3

Q3. A traditional VLIW processor accepts long instructions that have the following five fields:

Branch	ALII	ALII	Memory	Memory
Dianch	ALU	ALU	Wichioi y	Wichioi y

Show the best schedule for the following operations into such 5-operation instructions. Assume that the processor has full forwarding paths, branch and ALU instructions are executed in one cycle, and memory instructions are executed in two cycles.

```
lw r1, 0(r2)
lw r3, 4(r2)
add r1, r1, r3
sw r1, 8(r2)
```

Branch	ALU	ALU	Memory	Memory
nop	nop	nop	lw	lw
nop	nop	nop	nop	nop
nop	add	nop	nop	nop
nop	nop	nop	sw	nop