## Quiz 1A



Instructions: Time 15 minutes. Open book and notes exam. No electronics. Please answer all problems in the space provided and limit your answer to the space provided. No questions are allowed.

P1. According to Moore's Law, the quantity of transistors on a single chip doubles approximately every two years. If the current leading CPU chip contains 50 billion transistors, what is the projected maximum number of transistors anticipated on a processor chip in eight years?
<2.5 marks>

In 8 years, there are four doubling intervals.
Therefore,
Transistors/chip $=50 \times 2^{4}=800$ billion transistors

P2. Consider a 5-stage pipelined processor discussed in class that resolves data hazards by introducing stalls. The only forwarding mechanism available is through the Register File, where results written can be read in the same cycle. Utilize the multi-cycle pipeline diagram provided below to illustrate how this processor processes the given instruction sequence.
<2.5 marks>

|  | Instruction | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| add | x1,x2,x3 | F | D | E | M | W |  |  |  |  |  |  |  |  |  |  |
| sub | x4, x1, x5 |  | F | D | D | D | E | M | W |  |  |  |  |  |  |  |
| add | $x 5, x 4, x 7$ |  |  | F | F | F | D | D | D | E | M | W |  |  |  |  |
|  | x1,0 (x4) |  |  |  |  |  | F | F | F | D | E | M | W |  |  |  |

[^0]
[^0]:    <Good Luck>

