Instructions: Time 15 minutes. Open book and notes exam. No electronics. Please answer all problems in the space provided and limit your answer to the space provided. No questions are allowed.

P1. Complete the following table based on your understanding of Moore's Law.

| Year | Transistors/chip |
| :---: | :---: |
| $x$ | 15 billion |
| $x+2$ | 30 billion |
| $x+6$ | $\mathbf{1 2 0}$ billion |

From $x$ to $x+2$, there is doubling in two years.
From $x+2$ to $x+6$, there are two doubling intervals.
Therefore,
Transistors/chip $=30 \times 2^{2}=120$ billion

P2. Assume that the following RISC-V instruction sequence is executed on a dual-issue superscalar processor that features dynamic scheduling and speculation using reservation stations and reorder buffer like what you have learned in the class. Assume that this processor has two integer execution units, one address calculation unit, one memory port, and many reservation stations and reorder buffer entries. Use the pipeline diagram below to show how this processor executes the instruction sequence shown.

|  | Instruction | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| add | $\mathrm{x} 1, \mathrm{x} 2, \mathrm{x} 3$ | F | I | E | W | C |  |  |  |  |  |  |  |  |  |  |
| sub | $\mathrm{x} 4, \mathrm{x} 1, \mathrm{x} 5$ | F | I |  |  | E | W | C |  |  |  |  |  |  |  |  |
| ld | x1,0(x4) |  | F | 1 |  |  |  | A | M | W | C |  |  |  |  |  |
| add | $x 5, x 4, x 7$ |  | F | I |  |  |  | E | W |  | C |  |  |  |  |  |

$<$ Good Luck>

