0907432 Computer Architecture and Organization 2 (Spring 2022)

Quiz 2B

الاسم: رقم التسجيل:

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Instructions: Time **10** minutes. Open book and notes exam. No electronics. Please answer all problems in the space provided and limit your answer to the space provided. No questions are allowed.

P1. Assume that you have a two-way associative cache with the following specifications: 4 sets, block size = 16 bytes, word size = 4 bytes, address width = 16 bits, and least recently used replacement policy. Similar to the example given in the class, complete the following table for the access sequence shown. *Note that the shown addresses are byte addresses in hexadecimal*.

Byte Addr.	Block Addr.	Cache Index	Hit/ Miss	Set 0		Set 1		Set 2		Set 3	
0x04	0	0	Miss	M[0]							
0x60	6	2	Miss	M[0]				M[6]			
0x88	8	0	Miss	M[0]	M[8]			M[6]			
0xC4	C	0	Miss	M[C]	M[8]			M[6]			
0x64	6	2	Hit	M[C]	M[8]			M[6]			
0x84	8	0	Hit	M[C]	M[8]			M[6]			
0x00	0	0	Miss	M[0]	M[8]			M[6]			

<Good Luck>