

**Instructions:** Time 60 minutes. Open book and notes exam. No electronics. Please answer all problems in the space provided and limit your answer to the space provided. There are six problems and each problem is for 5 marks.

<Good Luck>

**P1.** Suppose we have two implementations of the same instruction set architecture. Computer A has a clock rate of 3.0 GHz and a CPI of 1.5 for some program, and Computer B has a clock rate of 4.5 GHz and a CPI of 3.0 for the same program. Which computer is faster for this program and by how much?

**Solution:**

**CPU time = IC × CPI / f**

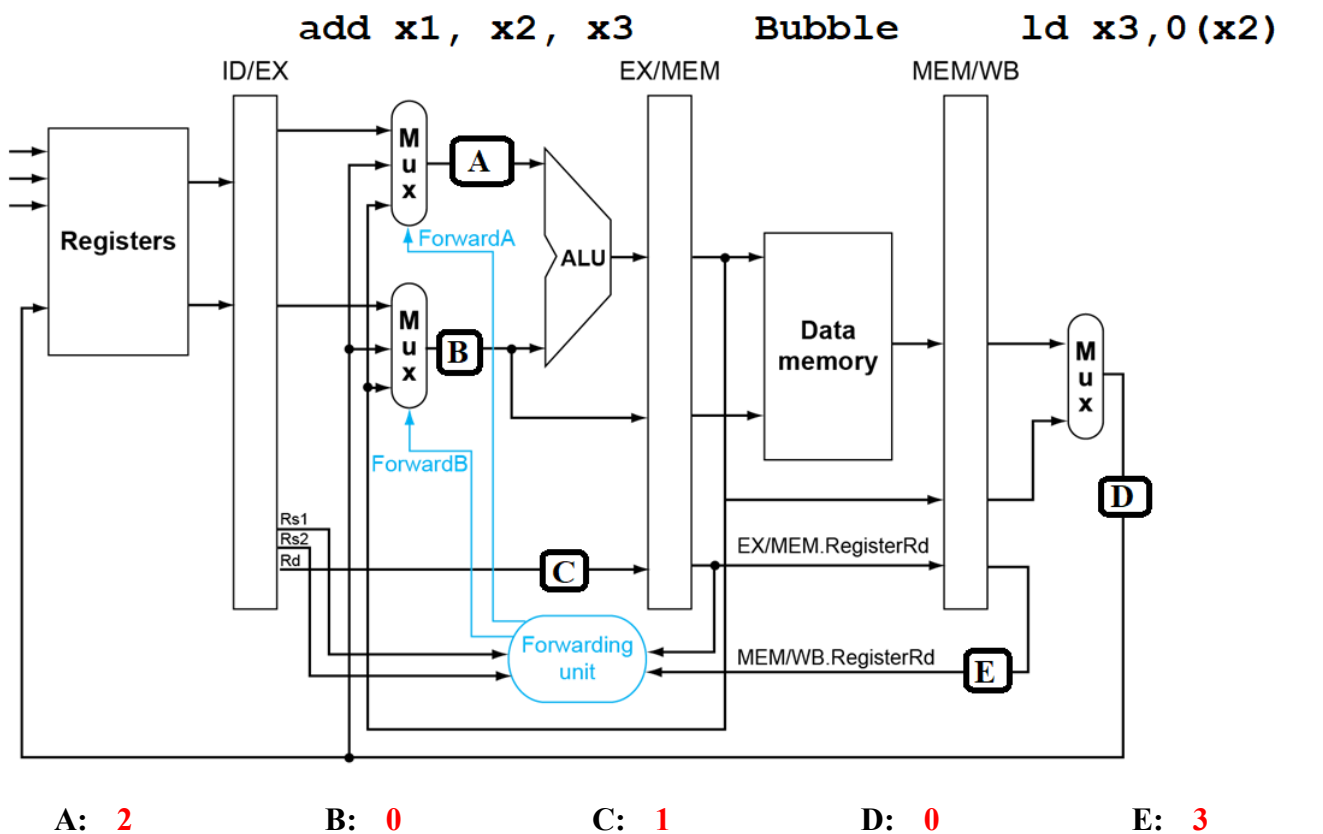
**Assume the instruction count is I**

**CPU time<sub>A</sub> = I × 1.5 / 3.0 GHz = I/2 ns**

**CPU time<sub>B</sub> = I × 3.0 / 4.5 GHz = 2I/3 ns**

**A is faster by (2I/3) / (I/2) = 4/3 times**

**P2.** With reference to the RISC-V pipeline with forwarding studied in the class, what are the decimal values on the busses A, B, C, D, and E? Assume that the **add** and **ld** instructions shown in the diagram below are in the execute and write-back stages, respectively. Also, assume that the contents of registers **x1**, **x2**, and **x3** are 1, 2, and 3, respectively, and all memory locations contain zeros.



**P3.** Assume that the following loop is executed by a speculative pipelined processor of degree 2. This processor uses reservation stations, common data buses, and reorder buffer. The fetch stage takes one cycle, and the issue stage takes one cycle. The multiply execution takes three cycles, integer/branch takes one cycle, and load takes two cycles (1 cycle for address calculation and 1 cycle for data memory access). The processor has one address calculation unit, one memory access unit, one integer ALU unit, and one branch unit. Assume also that branch prediction is used, and the branch instruction is predicted correctly as taken at the end of the first iteration. Use the multi-cycle pipeline diagram below to specify the execution of the loop's first iteration and the loop's first instruction of the second iteration.

```

LOOP: ld    x10, 0(x13)
      ld    x11, 8(x13)
      mul   x12, x10, x11
      add   x14, x14, x10
      subi  x13, x13, 16
      bnez  x12, LOOP
  
```

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
LOOP: ld x10, 0(x13)	F	I	A	M	W	C									
ld x11, 8(x13)	F	I		A	M	W	C								
mul x12, x10, x11		F	I				E	E	E	W	C				
add x14, x14, x10		F	I			E	W				C				
subi x13, x13, 16			F	I	E	W						C			
bnez x12, LOOP			F	I							E	W	C		
LOOP: ld x10, 0(x13)				F	I		A	M	W				C		

**P4.** Assume that you have a hard disk with the following specifications: 15,000 rpm, 4-ms average seek time, 8-ms maximum seek time, 0-ms controller overhead, and idle disk. What are the minimum and maximum times in milliseconds required to read one complete cylinder?

**The solution is:**

**Minimum time = rotation time =  $60 / 15,000 = 4$  ms**

**Maximum time = max seek time + max rotational latency + rotation time  
=  $8 + 4 + 4 = 16$**

**P5.** Unroll the following loop three times and use the table below to schedule the unrolled loop efficiently for the static dual-issue processor described in the class.

```

Loop:  addi x1,x1,1           // increment value in x1
       sd  x1,0(x20)        // store the value
       addi x20,x20,-8      // decrement pointer
       blt x22,x20,Loop     // branch if x22 < x20
    
```

	ALU/branch	Load/store	Cycle
<b>Loop:</b>	<b>addi x1,x1,1</b>		1
	<b>addi x20,x20,-24</b>	<b>sd x1,0(x20)</b>	2
	<b>addi x1,x1,1</b>		3
	<b>addi x1,x1,1</b>	<b>sd x1,16(x20)</b>	4
	<b>blt x22,x20,Loop</b>	<b>sd x1,8(x20)</b>	5
			6
			7

**P6.** A DDR3-SDRAM chip has 8 memory array banks, and each array is 32,768 rows and 128 columns. What is the chip's capacity in Gbits given that each array cell is 128 bits?

**The solution is:**

$$\begin{aligned}
 \text{Size} &= \text{Banks} * \text{Rows} * \text{Columns} * \text{Cell size} \\
 &= 8 * 32,768 * 128 * 128 \\
 &= 2^3 * 2^5 * 2^{10} * 2^7 * 2^7 \\
 &= 2^{32} \\
 &= 4 \text{ Gbits}
 \end{aligned}$$