

Quiz 1B

رقم الشعبة الأصلية:

رقم التسجيل:

الاسم:

Instructions: Time 15 minutes. Open book and notes exam. No electronics. Please answer all problems in the space provided and limit your answer to the space provided. No questions are allowed.

P1. What is the main approach computer engineers are currently using to develop new processors with higher performance?

Having more cores on the processor chip

P2. A processor runs on a 4.0-GHz clock. What is the CPU execution time of a program that has the following instruction mix?

- 2×10^{10} instruction with average cycles per instruction of 1.0.
- 3×10^{10} instruction with average cycles per instruction of 2.0.

$$\begin{aligned} \text{Time} &= \sum (IC_i \times CPI_i) / f \\ &= (2 \times 10^{10} \times 1.0 + 3 \times 10^{10} \times 2.0) / 4 \times 10^9 \\ &= 80 / 4 = 20 \text{ sec} \end{aligned}$$

P3. Use multicycle pipeline diagram to show the execution of the following code sequence on a speculative pipeline processor of degree 4. This processor uses reservation stations, common data buses, and reorder buffer. The fetch stage takes one cycle, and the issue stage takes one cycle. The integer/branch latency is 1 cycle, and the load latency is 2 cycles (1 cycle for address calculation and 1 cycle for data memory access). The processor has two address calculation units, two memory access units, three integer ALU units, and one branch unit.

| Instruction | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
|------------------|---|---|---|---|---|---|---|---|---|----|----|----|----|----|----|
| addi x30, x10, 8 | F | I | E | W | C | | | | | | | | | | |
| addi x31, x10, 0 | F | I | E | W | C | | | | | | | | | | |
| sd x31, 0(x30) | F | I | | | A | C | | | | | | | | | |
| ld x30, 0(x30) | F | I | | | A | | M | W | C | | | | | | |
| add x5, x30, x31 | | F | I | | | | | | E | W | C | | | | |
| sd x5, 0(x11) | | F | I | A | | | | | | | C | | | | |

<Good Luck>