## Chapter 1

## Computer Abstractions and Technology

Adapted by Prof. Gheith Abandah

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1.2 Seven Great Ideas in Computer Architecture (Review)
1.5 Technologies for Building Processors and Memory
1.6 Performance (Review)
1.7 The Power Wall
1.8 The Sea Change: The Switch from Uniprocessors to Multiprocessors
1.9 Real Stuff: Benchmarking the Intel Core i7
1.10 Fallacies and Pitfalls
1.11 Concluding Remarks

## Seven Great Ideas

- Use abstraction to simplify design
- Make the common case fast
- Performance via parallelism
- Performance via pipelining
- Performance via prediction
- Hierarchy of memories
- Dependability via redundancy



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## Technology Trends

42 Years of Microprocessor Trend Data


Original data up to the year 2010 collected and plotted by M. Horowitz, F. Labonte, O. Shacham, K. Olukotun, L. Hammond, and C. Batten New plot and data collected for 2010-2017 by K. Rupp

## Technology Trends



FIGURE 1: The Dennard scaling failed around the middle of the 2000s [24].

## Technology Trends

Electronics technology continues to evolve

- Increased capacity and performance
- Reduced cost


| Year | Technology | Relative performance/cost |
| :--- | :--- | ---: |
| 1951 | Vacuum tube | 1 |
| 1965 | Transistor | 35 |
| 1975 | Integrated circuit (IC) | 900 |
| 1995 | Very large scale IC (VLSI) | $2,400,000$ |
| 2013 | Ultra large scale IC | $250,000,000,000$ |

## Semiconductor Technology

Silicon: semiconductor
Add materials to transform properties:

- Conductors
- Insulators
- Switch
- YouTube Video: VLSI Fabrication Process


## https://youtu.be/fwNkg1fsqBY

## Manufacturing ICs



- Yield: proportion of working dies per wafer


## Intel Core $\mathbf{1 0}^{\text {th }}$ Gen



- 300mm wafer, 506 chips, 10 nm technology
- Each chip is $11.4 \times 10.7 \mathrm{~mm}$


## Integrated Circuit Cost

Cost per die $=\frac{\text { Cost per wafer }}{\text { Dies per wafer } \times \text { Yield }}$
Dies per wafer $\approx$ Wafer area/Die area
Yield $=\frac{1}{(1+(\text { Defectsper area } \times \text { Die area/2 }))^{2}}$

- Nonlinear relation to area and defect rate
- Wafer cost and area are fixed
- Defect rate determined by manufacturing process
- Die area determined by architecture and circuit design


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## Response Time and Throughput

## Response time

- How long it takes to do a task

Throughput

- Total work done per unit time
- e.g., tasks/transactions/... per hour
- How are response time and throughput affected by
- Replacing the processor with a faster version?
- Adding more processors?
- We'll focus on response time for now...


## Relative Performance

Define Performance $=1 /$ Execution Time
" X is $n$ time faster than $Y$ "
Performanœ $_{X} /$ Performan@ $_{Y}$
$=$ Execution time $_{\mathrm{Y}} /$ Execution time $_{\mathrm{X}}=n$
Example: time taken to run a program

- 10s on A, 15 s on B
- Execution Time ${ }_{B}$ / Execution Time ${ }_{A}$
$=15 \mathrm{~s} / 10 \mathrm{~s}=1.5$
- So $A$ is 1.5 times faster than $B$


## Measuring Execution Time

Elapsed time

- Total response time, including all aspects

Processing, I/O, OS overhead, idle time

- Determines system performance
- CPU time
- Time spent processing a given job
- Discounts I/O time, other jobs' shares
- Comprises user CPU time and system CPU time
- Different programs are affected differently by CPU and system performance


## CPU Clocking

- Operation of digital hardware governed by a constant-rate clock

- Clock period: duration of a clock cycle
- e.g., 250 ps $=0.25 \mathrm{~ns}=250 \times 10^{-12} \mathrm{~s}$
- Clock frequency (rate): cycles per second
- e.g., $4.0 \mathrm{GHz}=4000 \mathrm{MHz}=4.0 \times 10^{9} \mathrm{~Hz}$


## CPU Time

## CPU Time $=$ CPU Clock Cycles $\times$ Clock Cycle Time <br> $$
=\frac{\text { CPU Clock Cycles }}{\text { ClockRate }}
$$

- Performance improved by
- Reducing number of clock cycles
- Increasing clock rate
- Hardware designer must often trade off clock rate against cycle count


## Instruction Count and CPI

Clock Cycles $=$ Instruction Count $\times$ Cycles per Instruction

$$
\begin{aligned}
\text { CPU Time } & =\text { Instruction Count } \times \mathrm{CPI} \times \text { Clock Cycle Time } \\
& =\frac{\text { Instruction Count } \times \mathrm{CPI}}{\text { Clock Rate }}
\end{aligned}
$$

- Instruction Count for a program
- Determined by program, ISA and compiler
- Average cycles per instruction
- Determined by CPU hardware
- If different instructions have different CPI
- Average CPI affected by instruction mix


## CPI in More Detail

- If different instruction classes take different numbers of cycles

$$
\text { Clock Cycles }=\sum_{i=1}^{n}\left(\text { CPI }_{i} \times \text { Instruction Count }{ }_{i}\right)
$$

- Weighted average CPI

$$
\mathrm{CPI}=\frac{\text { Clock Cycles }}{\text { Instruction Count }}=\sum_{\mathrm{i}=1}^{\mathrm{n}}(\mathrm{CPI}_{\mathrm{i}} \times \underbrace{\text { Int }}_{\text {Relative frequency }_{\text {Instruction Count }}^{\text {Instruction Count }}})
$$

## Performance Summary

The BIC Pigture

$$
\text { CPU Time }=\frac{\text { Instructions }}{\text { Program }} \times \frac{\text { Clock cycles }}{\text { Instruction }} \times \frac{\text { Seconds }}{\text { Clock cycle }}
$$

- Performance depends on
- Algorithm: affects IC, possibly CPI
- Programming language: affects IC, CPI
- Compiler: affects IC, CPI
- Instruction set architecture: affects IC, CPI, $\mathrm{T}_{\mathrm{c}}$


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## Power Trends



## - In CMOS IC technology



## Reducing Power

Suppose a new CPU has

- $85 \%$ of capacitive load of old CPU
- $15 \%$ voltage and $15 \%$ frequency reduction

$$
\frac{P_{\text {new }}}{P_{\text {old }}}=\frac{C_{\text {old }} \times 0.85 \times\left(V_{\text {old }} \times 0.85\right)^{2} \times F_{\text {old }} \times 0.85}{C_{\text {old }} \times V_{\text {old }}{ }^{2} \times F_{\text {old }}}=0.85^{4}=0.52
$$

- The power wall
- We can't reduce voltage further
- We can't remove more heat

How else can we improve performance?

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## Uniprocessor Performance



## Uniprocessor Performance

40 years of Processor Performance


## Multiprocessors

- Multicore microprocessors
- More than one processor per chip
: Requires explicitly parallel programming
- Compare with instruction level parallelism
- Hardware executes multiple instructions at once
- Hidden from the programmer
- Hard to do
- Programming for performance
- Load balancing
- Optimizing communication and synchronization


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## SPEC CPU Benchmark

Programs used to measure performance

- Supposedly typical of actual workload
- Standard Performance Evaluation Corp (SPEC)
- Develops benchmarks for CPU, I/O, Web, ...
- SPEC CPU2017
- Elapsed time to execute a selection of programs

Negligible I/O, so focuses on CPU performance

- Normalize relative to reference machine
- Summarize as geometric mean of performance ratios
- CINT2017 (integer) and CFP2017 (floating-point)


## SPECspeed 2017 Integer benchmarks on a 1.8 GHz Intel Xeon E5-2650L

| Description | Name | Instruction Count $\times 10^{9}$ | CPI | Clock cycle time (seconds $\times 10^{-9}$ ) | Execution Time (seconds) | Reference Time (seconds) | SPECratio |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Perl interpreter | perlbench | 2684 | 0.42 | 0.556 | 627 | 1774 | 2.83 |
| GNU C compiler | gcc | 2322 | 0.67 | 0.556 | 863 | 3976 | 4.61 |
| Route planning | mcf | 1786 | 1.22 | 0.556 | 1215 | 4721 | 3.89 |
| Discrete Event simulation computer network | omnetpp | 1107 | 0.82 | 0.556 | 507 | 1630 | 3.21 |
| XML to HTML conversion via XSLT | xalancbmk | 1314 | 0.75 | 0.556 | 549 | 1417 | 2.58 |
| Video compression | x264 | 4488 | 0.32 | 0.556 | 813 | 1763 | 2.17 |
| Artificial Intelligence: alpha-beta tree search (Chess) | deepsjeng | 2216 | 0.57 | 0.556 | 698 | 1432 | 2.05 |
| Artificial Intelligence: <br> Monte Carlo tree <br> search (Go) | leela | 2236 | 0.79 | 0.556 | 987 | 1703 | 1.73 |
| Artificial Intelligence: recursive solution generator (Sudoku) | exchange2 | 6683 | 0.46 | 0.556 | 1718 | 2939 | 1.71 |
| General data compression | XZ | 8533 | 1.32 | 0.556 | 6290 | 6182 | 0.98 |
| Geometric mean | - | - | - | - | - | - | 2.36 |

## SPEC Power Benchmark

- Power consumption of server at different workload levels
- Performance: ssj_ops/sec
- Power: Watts (Joules/sec)

Overallssj_opsper Watt $=\left(\sum_{i=0}^{10}\right.$ ssj_ops $\left._{i}\right) /\left(\sum_{i=0}^{10}\right.$ power $\left._{i}\right)$

## SPECpower_ssj2008 for Xeon E5-2650L

| Target Load \% | Performance <br> (ssj_ops) | Average Power <br> (watts) |
| :---: | :---: | :---: |
| $100 \%$ | $4,864,136$ | 347 |
| $90 \%$ | $4,389,196$ | 312 |
| $80 \%$ | $3,905,724$ | 278 |
| $70 \%$ | $3,418,737$ | 241 |
| $60 \%$ | $2,925,811$ | 212 |
| $50 \%$ | $2,439,017$ | 183 |
| $40 \%$ | $1,951,394$ | 160 |
| $30 \%$ | $1,461,411$ | 141 |
| $20 \%$ | 974,045 | 128 |
| $10 \%$ | 485,973 | 115 |
| $0 \%$ | 0 | 48 |
| Overall Sum | $26,815,444$ | 2,165 |
| $\sum$ ssj_ops $/ \sum$ power $=$ |  | 12,385 |

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## Pitfall: Amdahl's Law

- Improving an aspect of a computer and expecting a proportional improvement in overall performance

$$
\mathrm{T}_{\text {improved }}=\frac{\mathrm{T}_{\text {affected }}}{\text { improvemen } \mathrm{t} \text { factor }}+\mathrm{T}_{\text {unaffected }}
$$

- Example: multiply accounts for 80s/100s
- How much improvement in multiply performance to get $5 \times$ overall?

$$
20=\frac{80}{n}+20 \quad \text { Can't be done }!
$$

- Corollary: make the common case fast


## Fallacy: Low Power at Idle

- Look back at i7 power benchmark
- At 100\% load: 258W
- At 50\% load: 170W (66\%)
- At 10\% load: 121W (47\%)
- Google data center
- Mostly operates at 10\% - 50\% load
- At $100 \%$ load less than $1 \%$ of the time
- Consider designing processors to make power proportional to load


## Pitfall: MIPS as a Performance Metric

MIPS: Millions of Instructions Per Second

- Doesn't account for

Differences in ISAs between computers

- Differences in complexity between instructions

$$
\begin{aligned}
\text { MIPS } & =\frac{\text { Instruction count }}{\text { Execution time } \times 10^{6}} \\
& =\frac{\text { Instruction count }}{\frac{\text { Instruction count } \times \mathrm{CPI}}{\text { Clock rate }} \times 10^{6}}=\frac{\text { Clock rate }}{\mathrm{CPI} \times 10^{6}}
\end{aligned}
$$

- CPI varies between programs on a given CPU


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## Concluding Remarks

Cost/performance is improving

- Due to underlying technology development

Execution time: the best performance measure Power is a limiting factor

- Use parallelism to improve performance

