0907731 Advanced Computer Architecture (Fall 2021)
Midterm Exam

الاسم: ..... رقم التسجيل: ..... رقم التسلسل: .....

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Instructions: Time **60** min. Open book and notes exam. No electronics. Please answer all problems in the space provided and limit your answer to the space provided. No questions are allowed. There are six problems, and each problem has 5 points.

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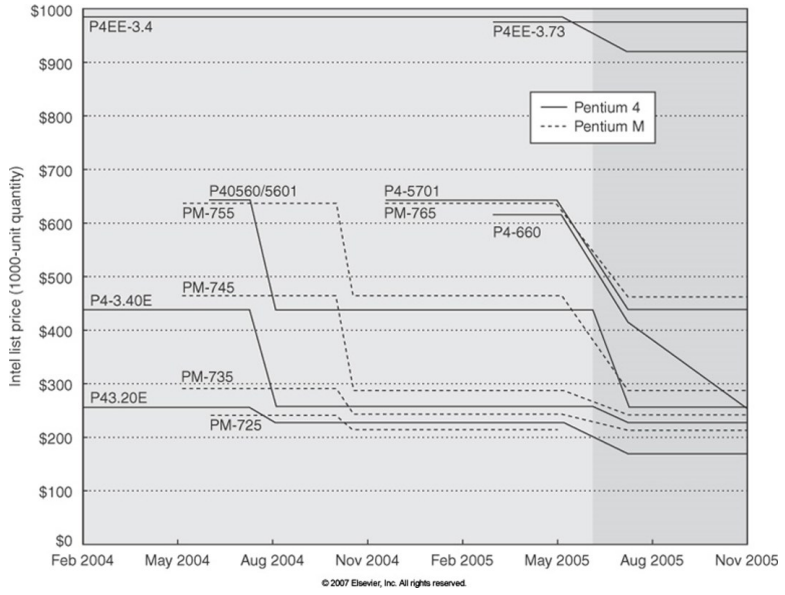
P1. The single processor performance improvement has slowed down after 2002. What are the main three reasons for this slowdown?

The solution:

1. **Increasing the processor clock rate further generates excessive heat that cannot easily be dissipated.**
2. **The available application instruction level parallelism is limited and is difficult to be exploited further.**
3. **Increasing the number of transistors on the processor chip is slowing.**

P2. Given the following graph that shows the change of processor price over time,



a) Why some processors are more expensive than others?

The solution:

More powerful processors have larger chips and are more expensive to design and manufacture.

b) Why prices fall in steps not steadily?

The solution:

Processor prices fall based on marketing decisions particularly when newer models are introduced and yield improves.

P3. Assume that you have a two-way associative cache with the following specifications: address width = 32 bits, size = 16 Kbytes, block size = 128 bits, and write back scheme.

a) How many sets does this cache have?

The solution is:

Number of sets = cache size / associativity / block size in bytes

= 16 KB / 2 / (128/8)

= 512 sets

b) In addition to the data bits, what is the size of the other bits that each block has (e.g., tag, valid)?

The solution:

<block offset> = $\lg_2$ (block size in bytes) = $\lg_2$ (128/8) = 4 bits

<index> = $\lg_2$ (No. of sets) = $\lg_2$ (512) = 9 bits

<tag> = 32 - <index> - <block offset> = 32 – 4 – 9 = 19 bits

Total additional bits = <tag> + valid bit + dirty bit = 21 bits

P4. Assume that you have a 4 Gbit DDR3-1600 SDRAM chip that has data width of 8 bits.

a) How many rows does this chip has knowing that it has 1024 columns in each of its 8 banks?

The solution is:

Number of locations = Size / data width = 4 Gbit / 8 bits = 512 M

Number of rows = Number of locations / banks / columns

= 512 M / 8 / 1024 = 512 K / 8 = 64 K rows

b) What is its peak transfer rate in bytes per second?

The solution:

Peak transfer rate = 1600 M transfers/sec * 1 byte

= 1600 Mbytes/sec

P5. Using the following multicycle pipeline diagram, show the execution of one iteration of the following RISC-V loop on the 5-stage pipeline studied in the class. Assume that the pipeline has all necessary forwarding paths, branch instructions are resolved in the decode stage without branch prediction, and the branch if not zero (`bnz`) instruction is not taken. Also show the execution of the instruction `I7` that comes after this loop.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
`Loop: lw x1,0(x2)`	***F***	***D***	***E***	***M***	***W***											
`addi x1,x1,1`		***F***	***D***	***D***	***E***	***M***	***W***									
`sw x1,0(x2)`			***F***	***F***	***D***	***E***	***M***	***W***								
`addi x2,x2,4`					***F***	***D***	***E***	***M***	***W***							
`sub x4,x3,x2`						***F***	***D***	***E***	***M***	***W***						
`bnz x4,Loop`							***F***	***D***	***D***	***E***	***M***	***W***				
`I7`										***F***	***D***	***E***	***M***	***W***		

P6. Assume that the following RISC-V loop is executed by a speculative pipelined processor. This processor uses reservation stations, common data bus, and reorder buffer. All stages take one cycle each. The processor has one address calculation unit, one memory access unit, two integer ALU units, one branch unit, and one FP unit. Using the multi-cycle pipeline diagram below, specify the execution of these instructions in this processor pipeline. Assume that the branch is correctly predicted as a taken branch. Note that the last instruction below is the first instruction of the loop's second iteration.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
`Loop: lw x1,0(x2)`	***F***	***I***	***A***	***M***	***W***	***C***										
`addi x1,x1,1`		***F***	***I***			***E***	***W***	***C***								
`sw x1,0(x2)`			***F***	***I***	***A***				***C***							
`addi x2,x2,4`				***F***	***I***	***E***		***W***		***C***						
`sub x4,x3,x2`					***F***	***I***			***E***	***W***	***C***					
`bnz x4,Loop`						***F***	***I***				***E***	***W***	***C***			
`lw x1,0(x2)`							***F***	***I***	***A***	***M***	***W***			***C***		

<Good Luck>