



<b>Course</b>	Computer Architecture and Organization (2) – 0917432 (3 Cr. – Core Course)
<b>Catalog Description</b>	Exploiting instruction level parallelism, hardware and software approaches. Pipelined, Vector, Super scalar, and VLIW processors. Predication, Branch Prediction, and Control and Data Speculation. Case Studies of Modern Processors. Hierarchical Memory Design. Virtual memory. Input/Output Interfacing and System Integration. Introduction to Parallel Processing. Flynn’s classification. Symmetric Multiprocessors. Cache coherence.
<b>Prerequisites by Course</b>	Computer Architecture and Organization (1) – (0917335)
<b>Prerequisites by Topic</b>	Students are assumed to have had sufficient knowledge pertaining to digital logic design, RISC-V instruction set architecture, computer arithmetic, processor datapath and control design, single-cycle, multi-cycle, and pipelined implementations of processors.
<b>Textbook</b>	Patterson and Hennessy. Computer Organization & Design: The Hardware/Software Interface, RISC-V ed., Morgan Kaufmann, Elsevier Inc., 2018.
<b>References</b>	<ol style="list-style-type: none"><li>1. Hennessy and Patterson, Computer Architecture: A Quantitative Approach, 6th ed., Morgan Kaufmann, Elsevier Inc., 2017.</li><li>2. J. P. Shen and M. H. Lipasti. Modern Processor Design: Fundamentals of Superscalar Processors, Mc Graw Hill, 2005.</li><li>3. D. Culler and J.P. Singh with A. Gupta. Parallel Computer Architecture: A Hardware/Software Approach, Morgan Kaufmann, 1998.</li><li>4. J. Hayes. Computer Architecture and Organization, 3rd ed., McGraw-Hill, 1998.</li></ol>
<b>Course Website</b>	<a href="http://www.abandah.com/gheith/?page_id=2671">http://www.abandah.com/gheith/?page_id=2671</a>
<b>Microsoft Teams</b>	<a href="#">Link</a>
<b>Schedule &amp; Duration</b>	15 Weeks, 43 lectures, 50 minutes each Or 31 lectures, 75 minutes each
<b>Student Material</b>	Textbook, class handouts, some instructor keynotes, and any additional reading assigned by the instructor.
<b>College Facilities</b>	Classroom with whiteboard and projection display facilities, library, and computer laboratory.
<b>Course Objectives</b>	The objectives of this course are: <ol style="list-style-type: none"><li>1. Introduce students to the technological changes in designing and building processors and computers.</li><li>2. Introduce students to the advanced techniques used in modern processors including pipelining, branch prediction, dynamic and speculative execution, multiple issue, multithreading, and software optimizations.</li><li>3. Introduce the students to the basic concepts and technologies used in designing memory and storage systems including cache, main memory, virtual memory, and secondary memory.</li></ol>

4. Introduce the students to the various approaches in parallel processing including SIMD extensions, vector processors, GPUs, multicore processors, shared memory multiprocessors, clusters, and message-passing multi-computers.

**Course Outcomes and Relation to ABET Program Outcomes**

Upon successful completion of this course, a student should be able to:

1. Understand and analyze the performance of single-processor architectures, as well as multiprocessor architectures [1].
2. Understand and analyze the performance of memory hierarchy levels [1].
3. Understand the technological improvements and the effect of these improvements on modern computers [4].
4. Survey research papers that describe contemporary issues in computer design [3, 4, 7].

**Course Topics**

1. Introduction
2. Computer Technology and Performance (Sections 1.5–1.11)
3. Processor: Instruction-Level Parallelism (Sections 4.6–4.11, 4.14–4.15)
4. Memory Hierarchy (Sections 5.1–5.11, 5.13, 5.16–5.17)
5. Parallel Processors (Sections 6.1–6.8, 6.10–6.14)

**Computer Usage**

Practical aspects of the course are covered in Computer Design Lab 0907439.

**Important Dates**

Date	Event
Mon 22 Feb, 2021	First Lecture
TBA, 2021	Midterm Exam
Mon 24 May, 2021	Project Report Due
Sun 30 May, 2021	Last Date to Withdraw
Mon 31 May, 2021	Last Lecture
Jun 1 - 14, 2021	Final Exam Period

**Policies**

- Attendance is required. Class attendance will be taken every class and the university policies will be enforced in this regard.
- All submitted work must be yours
- Cheating will not be tolerated
- Open-book exams
- Check department announcements at:  
<http://www.facebook.com/pages/Computer-Engineering-Department/369639656466107> for general department announcements.

**Assessments**

Reports, participation, and exams

**Grading policy**

Participation	10%
Technology Trends Research Project	10%
Midterm Exam	30%
Final Exam	50%

**Instructors**

**Prof. Gheith Abandah**, [abandah@ju.edu.jo](mailto:abandah@ju.edu.jo)  
**Homepage:** <http://www.abandah.com/gheith>  
**Office Hours:** Sun through Thu: 8:00 am – 4:00 pm

**Class Time and Location**

Section 1: Mon and Wed: 10:00–11:30, CPE 102, [Microsoft Teams](#)

**Last Updated**

Feb 19, 2021

## Program Outcomes (PO)

<b>1</b>	an ability to identify, formulate, and solve complex engineering problems by applying principles of engineering, science, and mathematics
<b>2</b>	an ability to apply engineering design to produce solutions that meet specified needs with consideration of public health, safety, and welfare, as well as global, cultural, social, environmental, and economic factors
<b>3</b>	an ability to communicate effectively with a range of audiences
<b>4</b>	an ability to recognize ethical and professional responsibilities in engineering situations and make informed judgments, which must consider the impact of engineering solutions in global, economic, environmental, and societal contexts
<b>5</b>	an ability to function effectively on a team whose members together provide leadership, create a collaborative and inclusive environment, establish goals, plan tasks, and meet objectives
<b>6</b>	an ability to develop and conduct appropriate experimentation, analyze and interpret data, and use engineering judgment to draw conclusions
<b>7</b>	an ability to acquire and apply new knowledge as needed, using appropriate learning strategies.