

**0907432 Computer Design (Fall 2020)**  
**Homework 3**

**P1.** Assume you have a two-way set associative cache with four-word blocks and a total size of 32 words. Assume also that the cache is initially empty and uses true LRU replacement policy. For the following sequence of word-address references (not byte addresses), trace by completing the table below the behavior of the cache. For each reference, identify: the binary word address, the tag, the index, the word offset, whether the reference is a hit or a miss (compulsory, conflict or capacity), and which tags are in each way of the cache after the reference has been handled.

0x03, 0xb4, 0x2b, 0x02, 0xbe, 0x58, 0xbf, 0x0e, 0x1f, 0xbc

**4 words per block** → **2 bits for the word offset**  
**Number of blocks = 32 words / 4 = 8 blocks**  
**Number of sets = 8 blocks / 2 ways = 4 sets** → **2 bits for the index**

Word Address	Binary Address	Tag	Index	Word Offset	Hit/Miss	Miss Type	Way 0	Way 1
0x03	00000011	0	0	3	M	Comp.	T(0)=0 T(1)-- T(2)-- T(3)--	T(0)-- T(1)-- T(2)-- T(3)--
0xb4	10110100	b	1	0	M	Comp.	T(0)=0 T(1)=b T(2)-- T(3)--	T(0)-- T(1)-- T(2)-- T(3)--
0x2b	00101011	2	2	3	M	Comp.	T(0)=0 T(1)=b T(2)=2 T(3)--	T(0)-- T(1)-- T(2)-- T(3)--
0x02	00000010	0	0	2	H		T(0)=0 T(1)=b T(2)=2 T(3)--	T(0)-- T(1)-- T(2)-- T(3)--
0xbe	10111110	b	3	2	M	Comp.	T(0)=0 T(1)=b T(2)=2 T(3)=b	T(0)-- T(1)-- T(2)-- T(3)--
0x58	01011000	5	2	0	M	Comp.	T(0)=0 T(1)=b T(2)=2 T(3)=b	T(0)-- T(1)-- T(2)=5 T(3)--
0xbf	10111111	b	3	3	H		T(0)=0 T(1)=b T(2)=2 T(3)=b	T(0)-- T(1)-- T(2)=5 T(3)--
0x0e	00001110	0	3	2	M	Comp.	T(0)=0 T(1)=b T(2)=2 T(3)=b	T(0)-- T(1)-- T(2)=5 T(3)=0
0x1f	00011111	1	3	3	M	Comp.	T(0)=0 T(1)=b T(2)=2 T(3)=1	T(0)-- T(1)-- T(2)=5 T(3)=0
0xbc	10111100	b	3	0	M	Conf.	T(0)=0	T(0)--

							<b>T (1) =b</b>	T (1) =-
							T (2) =2	<b>T (2) =5</b>
							T (3) =1	<b>T (3) =b</b>

\* **Bold indicates most recently accessed way.**

**P2.** Draw a diagram that shows the TLB and cache interaction of a system with the following specifications: 32-bit virtual and physical addresses, 4-KB pages, 8-entry fully-associative TLB, and 4-way associative, physically-tagged, 16-Kbyte cache of 64-byte blocks. You must show the widths of all busses and the TLB and the cache hit circuits.

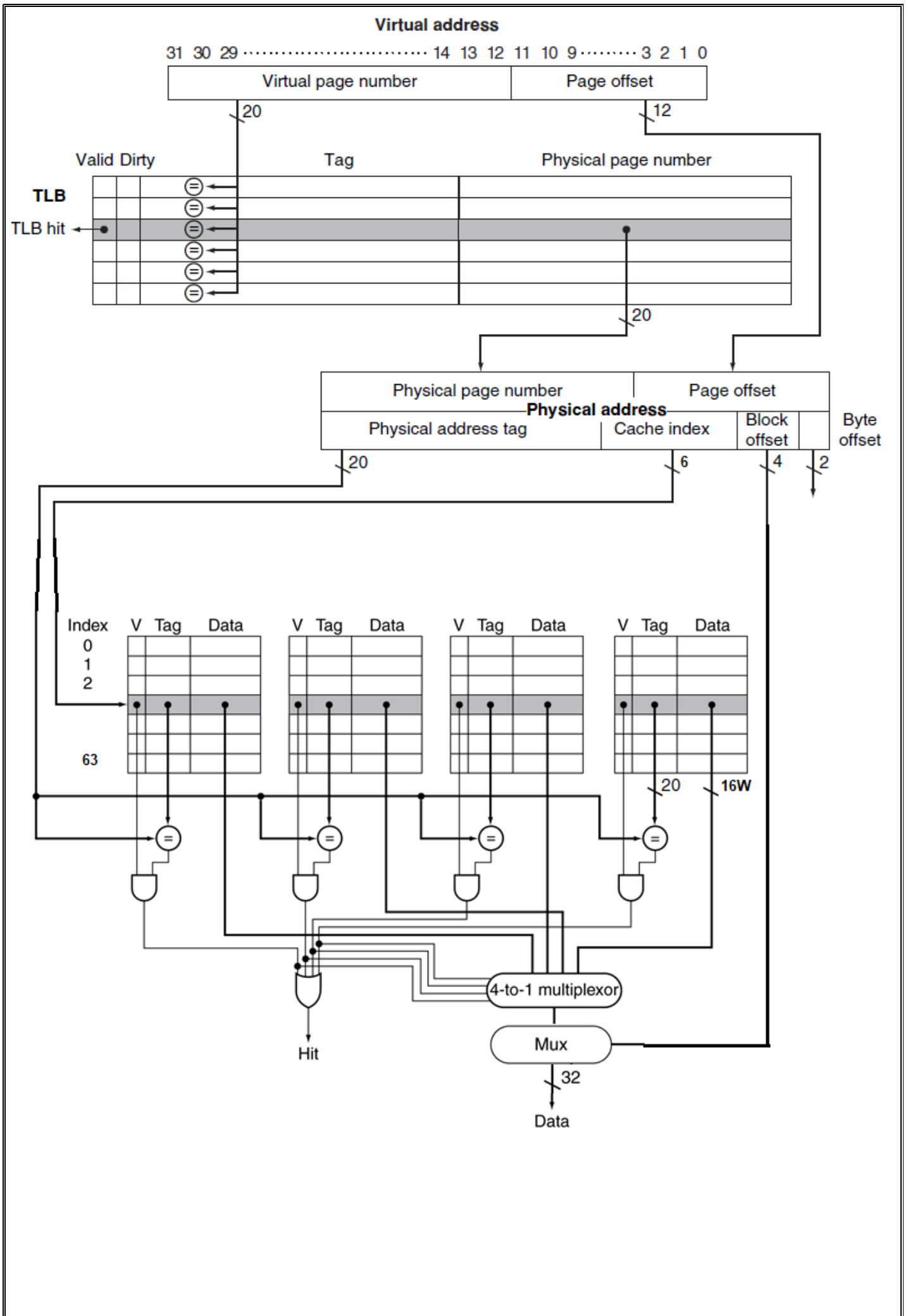
**<page offset> =  $\lg_2 4K = 12$  bits**

**<block offset> =  $\lg_2 64 = 6$  bits**

**Number of cache sets =  $16 \text{ Kbytes} / 64 \text{ bytes} / 4 \text{ ways} = 64$  sets**

**<index> =  $\lg_2 64 = 6$  bits**

**<tag> =  $32 - 6 - 6 = 20$  bits**



### P3. Dependability

- a) The following figure shows the parity bits, data bits, and field coverage in a Hamming ECC code for eight data bits. Assume that you have a memory module that uses this ECC code and that the binary sequence **110001000101** is read from the memory and it has a single bit error. What are the original eight data bits?

Bit position	1	2	3	4	5	6	7	8	9	10	11	12	
Encoded data bits	p1	p2	d1	p4	d2	d3	d4	p8	d5	d6	d7	d8	
Parity bit coverage	p1	X		X		X		X		X		X	
	p2		X	X			X	X			X	X	
	p4				X	X	X	X					X
	p8								X	X	X	X	X

123456789012  
110001000101  
ppdpdddpdddd

The data bits are 0010 0101

$p1 = \text{xor}(1\ 0\ 0\ 0\ 0\ 0) = 1$   
 $p2 = \text{xor}(1\ 0\ 1\ 0\ 1\ 0) = 1$   
 $p4 = \text{xor}(0\ 0\ 1\ 0\ 1) = 0$   
 $p8 = \text{xor}(0\ 0\ 1\ 0\ 1) = 0$

The error code is 0011 -> error in bit 3 (d1).

So the data is 1010 0101

- b) Who uses RAID 51 and why?

**Organizations that have branches in multiple locations use RAID 51. Compared with RAID 5, RAID 51 offers higher throughput, lower local latency, and higher redundancy and availability.**