Homework 3

P1. Assume you have a two-way set associative cache with four-word blocks and a total size of 32 words. Assume also that the cache is initially empty and uses true LRU replacement policy. For the following sequence of word-address references (not byte addresses), trace by completing the table below the behavior of the cache. For each reference, identify: the binary word address, the tag, the index, the word offset, whether the reference is a hit or a miss (compulsory, conflict or capacity), and which tags are in each way of the cache after the reference has been handled.

`0x03, 0xb4, 0x2b, 0x02, 0xbe, 0x58, 0xbf, 0x0e, 0x1f, 0xbc`

Word Address	Binary Address	Tag	Index	Word Offset	Hit/Miss	Miss Type	Way 0	Way 1
0x03	00000011	0	0	3	M	Comp.	**T(0)=0** T(1)=- T(2)=- T(3)=-	T(0)=- T(1)=- T(2)=- T(3)=-
0xb4								
0x2b								
0x02								
0xbe								
0x58								
0xbf								
0x0e								
0x1f								
0xbc								

* Bold indicates most recently accessed way.

P2. Draw a diagram that shows the TLB and cache interaction of a system with the following specifications: 32-bit virtual and physical addresses, 4-KB pages, 8-entry fully-associative TLB, and 4-way associative, physically-tagged, 16-Kbyte cache of 64-byte blocks. You must show the widths of all busses and the TLB and the cache hit circuits.

P3. Dependability

a) The following figure shows the parity bits, data bits, and field coverage in a Hamming ECC code for eight data bits. Assume that you have a memory module that uses this ECC code and that the binary sequence **110001000101** is read from the memory and it has a single bit error. What are the original eight data bits?

Bit position		1	2	3	4	5	6	7	8	9	10	11	12
Encoded data bits		p1	p2	d1	p4	d2	d3	d4	p8	d5	d6	d7	d8
Parity bit coverage	p1	X		X		X		X		X		X	
	p2		X	X			X	X			X	X	
	p4				X	X	X	X					X
	p8								X	X	X	X	X

b) Who uses RAID 51 and why?