0907432 Computer Design (Fall 2020)

Homework 2

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P1. The following loop is executed for 1,000 iterations.

```
Loop: ld   x10, 0(x13)
      ld   x11, 0(x14)
      mul  x12, x10, x11
      add  x16, x16, x12
      sd   x12, 0(x17)
      addi x17, x17, 8
      addi x14, x14, 8
      addi x13, x13, 8
      beq  x13, x12, Loop
```

a) Assume that this loop is executed on the five-stage RISC-V pipelined processor studied in the class. Assume also that this processor solves all data hazards through forwarding and stalls, resolves the branch instructions in the decode stage, and has one-cycle branch delay. How many cycles are needed to execute the 1,000 iterations ignoring the time needed to fill the pipeline?

```
                    1 2 3 4 5 6 7 8 9 0 1 2
ld   x10, 0(x13)    F D E M W
ld   x11, 0(x14)      F D E M W
mul  x12, x10, x11      F D D E M W
add  x16, x16, x12        F F D E M W
sd   x12, 0(x17)              F D E M W
addi x17, x17, 8                F D E M W
addi x14, x14, 8                  F D E M W
addi x13, x13, 8                    F D E M W
beq  x13, x12, Loop                   F D D E M W
ld   x10, 0(x13)                            F ...
```

From the pipeline diagram above, we see that it takes 12 cycles to finish one iteration and to start fetching instructions of the next iteration.
Also, time of one iterations = 9 instrs. + 2 stall cycles + 1 branch delay = 12 cycles
Total time = 12 × 1,000 = 12,000 cycles

b) Unroll this loop two times and schedule it for the static dual-issue processor studied in the class?
Performing replication, removing loop overhead, modifying instructions, and register renaming:

```
Loop: ld   x10, 0(x13)
      ld   x11, 0(x14)
      mul  x12, x10, x11
      add  x16, x16, x12
      sd   x12, 0(x17)
      ld   x20, 8(x13)
      ld   x21, 8(x14)
      mul  x22, x20, x21
      add  x16, x16, x22
      sd   x22, 8(x17)
      addi x17, x17, 16
      addi x14, x14, 16
      addi x13, x13, 16
      beq  x13, x12, Loop
```

Scheduling:

	ALU/branch	Load/store	Cycle
Loop:	addi x17, x17, 16	ld x10, 0(x13)	1
	addi x14, x14, 16	ld x11, 0(x14)	2
	addi x13, x13, 16	ld x20, 8(x13)	3
	mul x12, x10, x11	ld x21, -8(x14)	4
	add x16, x16, x12		5
	mul x22, x20, x21	sd x12, -16(x17)	6
	add x16, x16, x22		7
	beq x13, x12, Loop	sd x22, -8(x17)	8

c) Assuming same conditions as in (a) above, how many cycles are needed to execute the unrolled loop on the dual-issue processor?

It takes 8 cycles to issue two iterations.

Total time = (8+1) × (1,000 ÷ 2) = 4,500 cycles

P2. Assume that the following loop is executed by a speculative pipelined processor of degree 3. This processor uses reservation stations, common data buses, and reorder buffer. The fetch stage takes one cycle and the issue stage takes one cycle. The integer/branch latency is 1 cycle and the load latency is 2 cycles (1 cycle for address calculation and 1 cycle for data memory access). The processor has two address calculation units, two memory access units, two integer ALU units, and one branch unit.

```
Loop: ld   x10, 0(x13)
      ld   x11, 0(x14)
      mul  x12, x10, x11
      add  x16, x16, x12
      sd   x12, 0(x17)
      addi x17, x17, 8
      addi x14, x14, 8
      addi x13, x13, 8
      beq  x13, x12, Loop
```

a) Assume that branch prediction is used and the branch instruction is predicted wrongly as not taken at the end of the first iteration. Draw the multi-cycle pipeline diagram for the execution of the first two iterations of this loop to find how many cycles are needed to fetch and commit the two iterations.

```
                      1 2 3 4 5 6 7 8 9 0 1 2 3 4 5 6 7 8 9 0 1 2
ld   x10, 0(x13)      F I A M W C
ld   x11, 0(x14)      F I A M W C
mul  x12, x10, x11    F I       E W C
add  x16, x16, x12      F I         E W C
sd   x12, 0(x17)        F I A           C
addi x17, x17, 8        F I E W         C
addi x14, x14, 8          F I E W         C
addi x13, x13, 8          F I E W         C
beq  x13, x12, Loop       F I     E W     C
I10                         F . . .         n
. . .
ld   x10, 0(x13)                            F I A M W C
ld   x11, 0(x14)                            F I A M W C
mul  x12, x10, x11                          F I       E W C
add  x16, x16, x12                            F I         E W C
sd   x12, 0(x17)                              F I A           C
addi x17, x17, 8                              F I E W         C
addi x14, x14, 8                                F I E W         C
addi x13, x13, 8                                F I E W         C
beq  x13, x12, Loop                             F I     E W     C
```

22 cycles for two iterations.

b) Now assume that this processor has perfect branch prediction with no branch delay. Estimate the number of cycles needed to execute 1,000 iterations of this loop ignoring the time needed to fill the pipeline? (Show your work clearly)

```
                      1 2 3
ld   x10, 0(x13)      F I A M W C
ld   x11, 0(x14)      F I A M W C
mul  x12, x10, x11    F I       E W C
add  x16, x16, x12      F I         E W C
sd   x12, 0(x17)        F I A           C
addi x17, x17, 8        F I E W         C
addi x14, x14, 8          F I E W         C
addi x13, x13, 8          F I E W         C
beq  x13, x12, Loop       F I     E W     C
ld   x10, 0(x13)            F I A M W       C
ld   x11, 0(x14)            F I A M W       C
mul  x12, x10, x11          F I       E W   C
add  x16, x16, x12            F I         E W C
sd   x12, 0(x17)              F I A           C
addi x17, x17, 8              F I E W         C
addi x14, x14, 8                F I E W         C
addi x13, x13, 8                F I E W         C
beq  x13, x12, Loop             F I     E W     C
```

3 cycles are needed to fetch and issue each iteration.
Total time = 3 × 1,000 = 3,000 cycles