Form 1

4.Given the following execution times in seconds of three benchmarks (B1, B2, and B3) on a reference computer and a computer under test. What is the geometric mean of the relative performance (approximated to one decimal point)?
- Reference computer: 10 for B1, 15 for B2, 12 for B3
- Computer under test: 5 for B1, 10 for B2, 4 for B3

(5 Points)

- (•) 2.1
- ( ) 2.0
- ( ) 2.2
- ( ) 1.9
- ( ) 1.8

5.Assume that you have a five-stage pipelined processor similar to the one studied in the class. This processor has no forwarding paths to the execution stage and resolves data hazards through stalls. But as usual, data written in the register file in the first half of a cycle can be read in the second half on the same cycle. How many cycles are needed to fetch and complete execution the following five RISC-V instructions?

```
sub x2, x1, x3
and x12, x2, x5
or x13, x6, x2
add x14, x2, x2
sd x15, 100(x14)
```

(5 Points)

- ( ) 10 cycles
- ( ) 11 cycles
- ( ) 12 cycles
- (•) 13 cycles
- ( ) None of the other options

6.A processor has a 2-bit branch history table. The size of this table is 8K bits. How many address bits are needed to access this table?

(5 Points)

- (•) 12 bits
- ( ) 13 bits
- ( ) 14 bits
- ( ) 11 bits
- ( ) None of the other options

7.Assume that the following code sequence is executed by a dynamic quad-issue pipelined processor. This processor uses reservation stations, reorder buffer, and four common data

buses to execute the instructions out of order. The fetch stage takes one cycle and the issue stage takes one cycle. The integer latency is 1 cycle, and the memory latency is 2 cycles (1 cycle for address calculation and 1 cycle for data memory access). The processor has two address calculation units, two memory access units, and two integer ALU units. How many cycles are needed to fetch and complete execution of the following eight RISC-V instructions?

ld x1, 8(x2)
sd x3, 0(x1)
sub x11, x3, x1
and x12, x4, x11
add x7, x5, x6
sub x8, x5, x6
sub x13, x4, x4
and x14, x11, x3

(5 Points)

- 8 cycles
- 9 cycles
- 10 cycles
- 11 cycles
- None of the other options

8.A DDR2-SDRAM chip has four banks. Each bank is organized as 16K rows by 8K columns array with a data width of 16 bits. What is the capacity of this chip?

(5 Points)

- 512 Mbits
- 1 Gbits
- 2 Gbits
- 4 Gbits
- None of the other options

9.Assume that you have an 8-way set associative cache that has 1K sets with 64-byte blocks. What is the tag field width if the address width is 64 bits?

(5 Points)

- 48 bits
- 45 bits
- 54 bits
- 42 bits
- None of the other options

10.Assume that you have a computer that has a 32-bit virtual address and 64-KB pages. Given the contents of the shown fully-associative TLB, what is the translation of the virtual address 00010002 to physical address? (All numbers in this question are in hexadecimal)

No. V Tag Physical Page No.
==========
0 1 0001 AAAA
1 1 0002 BBBB
2 1 2000 CCCC
3 1 0000 DDDD
4 1 0003 EEEE
(5 Points)

- (•) AAAA0002
- ( ) BBBB0001
- ( ) 0002AAAA
- ( ) 0001BBBB
- ( ) None of the other options

11.To have a speedup of 10 using 16 processors, what should be the parallelizable fraction?
(5 Points)

- (•) 96%
- ( ) 4%
- ( ) 62.5%
- ( ) 37.5%
- ( ) None of the other options

12.What is the peak performance in Giga floating-point operations per second (GFLOPs/sec) for a processor that has the following double-precision floating-point specifications?
- 32 cores
- 4.0 GHz clock
- Has two 512-bit SIMD units
- Supports pipelined fused multiply-add operations

(5 Points)

- (•) 4096 GFLOPs/sec
- ( ) 2048 GFLOPs/sec
- ( ) 1024 GFLOPs/sec
- ( ) 512 GFLOPs/sec
- ( ) None of the other options

13.Assume that you have a hypercube interconnection network that connects 128 nodes. What is the maximum latency?
(5 Points)

- (•) 7 hops
- ( ) 6 hops
- ( ) 5 hops

- 8 hops
- None of the other options

Form 2

4.Given the following execution times in seconds of three benchmarks (B1, B2, and B3) on a reference computer and a computer under test. What is the geometric mean of the relative performance (approximated to one decimal point)?
- Reference computer: 10 for B1, 15 for B2, 12 for B3
- Computer under test: 5 for B1, 12 for B2, 4 for B3

(5 Points)

- 2.1
- 2.0
- 2.2
- 1.9
- 1.8

5.Assume that you have a five-stage pipelined processor similar to the one studied in the class. This processor has no forwarding paths to the execution stage and resolves data hazards through stalls. But as usual, data written in the register file in the first half of a cycle can be read in the second half on the same cycle. How many cycles are needed to fetch and complete execution the following five RISC-V instructions?

sub x2, x1, x3
and x12, x3, x5
or x13, x6, x2
add x14, x2, x2
sd x15, 100(x14)

(5 Points)

- 10 cycles
- 11 cycles
- 12 cycles
- 13 cycles
- None of the other options

6.A processor has a 2-bit branch history table. The size of this table is 4K bits. How many address bits are needed to access this table?

(5 Points)

- 12 bits
- 13 bits
- 14 bits
- 11 bits
- None of the other options

7.Assume that the following code sequence is executed by a dynamic quad-issue pipelined processor. This processor uses reservation stations, reorder buffer, and four common data

buses to execute the instructions out of order. The fetch stage takes one cycle and the issue stage takes one cycle. The integer latency is 1 cycle, and the memory latency is 2 cycles (1 cycle for address calculation and 1 cycle for data memory access). The processor has two address calculation units, two memory access units, and two integer ALU units. How many cycles are needed to fetch and complete execution of the following eight RISC-V instructions?

ld x1, 8(x2)
sd x3, 0(x1)
sub x11, x3, x1
and x12, x4, x1
add x7, x5, x6
sub x8, x5, x6
sub x13, x4, x4
and x14, x11, x3

(5 Points)

- 8 cycles
- 9 cycles
- 10 cycles
- 11 cycles
- None of the other options

8.A DDR2-SDRAM chip has four banks. Each bank is organized as 16K rows by 8K columns array with a data width of 8 bits. What is the capacity of this chip?

(5 Points)

- 512 Mbits
- 1 Gbits
- 2 Gbits
- 4 Gbits
- None of the other options

9.Assume that you have an 8-way set associative cache that has 8K sets with 64-byte blocks. What is the tag field width if the address width is 64 bits?

(5 Points)

- 48 bits
- 45 bits
- 54 bits
- 42 bits
- None of the other options

10.Assume that you have a computer that has a 32-bit virtual address and 64-KB pages. Given the contents of the shown fully-associative TLB, what is the translation of the virtual address 00020001 to physical address? (All numbers in this question are in hexadecimal)

No. V Tag Physical Page No.
==========
0 1 0001 AAAA
1 1 0002 BBBB
2 1 2000 CCCC
3 1 0000 DDDD
4 1 0003 EEEE
(5 Points)

- AAAA0002
- BBBB0001
- 0002AAAA
- 0001BBBB
- None of the other options

11.To have a speedup of 10 using 16 processors, what should be the serial fraction?
(5 Points)

- 96%
- 4%
- 62.5%
- 37.5%
- None of the other options

12.What is the peak performance in Giga floating-point operations per second (GFLOPs/sec) for a processor that has the following double-precision floating-point specifications?
- 32 cores
- 4.0 GHz clock
- Has two 256-bit SIMD units
- Supports pipelined fused multiply-add operations

(5 Points)

- 4096 GFLOPs/sec
- 2048 GFLOPs/sec
- 1024 GFLOPs/sec
- 512 GFLOPs/sec
- None of the other options

13.Assume that you have a hypercube interconnection network that connects 512 nodes. What is the maximum latency?
(5 Points)

- 7 hops
- 6 hops
- 5 hops

- 8 hops
- None of the other options

الامتحان النهائي التعويضي

4. أقسم بالله أنني لم أقدم أو أتلق أية مساعدة من أحد و لم أشهد أية حالة غش خلال هذا الامتحان ولم أخالف تعليمات هذا الامتحان

- أقسم
- لا أقسم

5.A processor runs on a 2-GHz clock, 1-volt power supply, and consumes 50 W dynamic power. What is the consumed dynamic power when the processor runs a turbo mode of 4 GHz and 1.4 volts?
(5 Points)

- 196 W
- 140 W
- 100 W
- 70 W
- None of the other options

6.Assume that you have a five-stage pipelined processor similar to the one studied in the class. This processor resolves data hazards through stalls and forwarding. However, it does not have forwarding paths to the execution stage from the memory stage. How many cycles are needed to fetch and complete execution the following five RISC-V instructions?
sub x2, x1, x3
and x12, x2, x5
or x13, x6, x2
add x14, x2, x2
sd x15, 100(x14)
(5 Points)

- 10 cycles
- 11 cycles
- 12 cycles
- 13 cycles
- None of the other options

7.A processor has a 128-entry branch target buffer. What is the approximate size of this buffer if the address width is 64 bits?
(5 Points)

- 512 bytes
- 1 Kbytes
- 2 Kbytes
- 256 bytes
- None of the other options

8.Assume that the following code sequence is executed by a dynamic dual-issue pipelined processor. This processor uses reservation stations, reorder buffer, and four common data buses to execute the instructions out of order. The fetch stage takes one cycle and the issue stage takes one cycle. The integer latency is 1 cycle, and the memory latency is 2 cycles (1 cycle for address calculation and 1 cycle for data memory access). The processor one address calculation unit, one memory access unit, and one integer ALU unit. How many cycles are needed to fetch and complete execution of the following eight RISC-V instructions?

ld x1, 8(x2)
sd x3, 0(x1)
sub x11, x3, x1
and x12, x4, x11
add x7, x5, x6
sub x8, x5, x6
sub x13, x4, x4
and x14, x11, x3

(5 Points)

- 12 cycles
- 13 cycles
- 14 cycles
- 11 cycles
- None of the other options

9.A DDR2-SDRAM chip has four banks and 4 Gbits capacity. What is the typical width of its address bus if its data width is 16 bits?

(5 Points)

- 14 bits
- 28 bits
- 16 bits
- 32 bits
- None of the other options

10.Assume that you have an 8-way set associative cache that has 1K sets with 64-byte blocks. What is the set index of the hexadecimal address 1234A438? (The answers below are in binary)

(5 Points)

- 1010010000
- 0000111000
- 0001001000110100
- 1001010010000
- None of the other options

11.Assume that you have the following four entries in a page table and you must replace one of the corresponding physical page. Which one you are likely to replace?
No. Valid Dirty Ref.
==========
0 1 0 0
1 0 0 0
2 1 1 0
3 1 0 1
(5 Points)

- The physical page of entry no. 0
- The physical page of entry no. 1
- The physical page of entry no. 2
- The physical page of entry no. 3
- None of the other options

12.Assume that the following loop is executed N iterations. How many vector RISC-V instructions are needed to executed this loop if N is less than the vector register width?

```
fld f0, a(x3)
addi x5, x19, 512
loop: fld f1, 0(x19)
fld f2, 0(x20)
fadd.d f1, f1, f2
fsd f1, 0(x19)
fmul.d f1, f0, f1
fsd f1, 0(x21)
addi x19, x19, 8
addi x20, x20, 8
addi x21, x21, 8
bltu x19, x5, loop
```

(5 Points)

- 5 vector instructions
- 6 vector instructions
- 7 vector instructions
- 8 vector instructions
- None of the other options

13.What is the arithmetic intensity of the following loop?

```
fld f0, a(x3)
addi x5, x19, 512
loop: fld f1, 0(x19)
fld f2, 0(x20)
fadd.d f1, f1, f2
fsd f1, 0(x19)
```

```
fmul.d f1, f0, f1
fsd f1, 0(x21)
addi x19, x19, 8
addi x20, x20, 8
addi x21, x21, 8
bltu x19, x5, loop
```

- 1 / 16
- 1 / 8
- 1 / 4
- 1 / 2
- None of the other options

14.Assume that you have a torus interconnection network that connects 256 nodes. What is the bisection bandwidth?
(5 Points)

- The bandwidth of 32 links
- The bandwidth of 16 blinks
- The bandwidth of 8 links
- The bandwidth of 256 links
- None of the other options