0907432 Computer Design (Spring 2020)
Homework

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Instructions: The deadline is **Sunday 3/5/2020 at 8:00 am**. There are six problems and each problem is for 2 marks. Please answer all problems with **clear handwriting**; typed answers are **not** acceptable. Each student must submit her/his own answers; submitting multiple similar answers is considered cheating and disciplinary actions will be taken. **Scan your answer sheets** using an appropriate smartphone app like Microsoft Office Lens. It is best that you assemble all your answer images in **one pdf file** and **email it to abandah@ju.edu.jo**. You must send your answers **from your university email** that ends @ju.edu.jo.

<Good Luck>

P1. A multicore processor has a clock rate of 3.0 GHz and voltage of 1.0 V. Assume that, on average, it consumes 75 W of static power and 30 W of dynamic power when all its six cores are active. It executes a program consisting of 10^{10} instructions on a single core with the following instruction mix.

Instruction Type	CPI	Frequency
Arithmetic	1.0	50%
Load/store	2.0	40%
Branch instructions	1.5	10%

a) Find the total execution time for this program on one core.
b) When this program is parallelized and run on the six cores, the number of arithmetic and load/store instructions per core is divided by 4, but the number of branch instructions remains the same. What is the execution time of the parallel program?
c) What is the speedup of the parallel program?
d) Assumes that the power consumed is proportional to the number of active cores. What are the energies consumed by the serial program on the single core and the parallel program on the six cores?
e) What is the average capacitive load of this processor when the six cores are active?
f) What is the average current drawn by this processor when the six cores are active?

P2. The following loop is executed for 1,000 iterations.

```
 Loop: ld    x10, 0(x13)
       ld    x11, 0(x14)
       mul   x12, x10, x11
       add   x16, x16, x12
       sd    x12, 0(x17)
       addi  x17, x17, 8
       addi  x14, x14, 8
       addi  x13, x13, 8
       beq   x13, x12, Loop
```

a) Assume that this loop is executed on the five-stage RISC-V pipelined processor studied in the class. Assume also that this processor solves all data hazards through forwarding and stalls, resolves the branch instructions in the decode stage, and has one-cycle branch delay. How many cycles are needed to execute the 1,000 iterations ignoring the time needed to fill the pipeline?
b) Unroll this loop two times and schedule it for the static dual-issue processor studied in the class?
c) Assuming same conditions as in (a) above, how many cycles are needed to execute the unrolled loop on the dual-issue processor?

P3. Assume that the following loop is executed by a speculative pipelined processor of degree 3. This processor uses reservation stations, common data buses, and reorder buffer. The fetch stage takes one cycle and the issue stage takes one cycle. The integer/branch latency is 1 cycle and the load latency is 2 cycles (1 cycle for address calculation and 1 cycle for data memory access). The processor has two address calculation units, two memory access units, two integer ALU units, and one branch unit.

```
Loop: ld    x10, 0(x13)
      ld    x11, 0(x14)
      mul   x12, x10, x11
      add   x16, x16, x12
      sd    x12, 0(x17)
      addi  x17, x17, 8
      addi  x14, x14, 8
      addi  x13, x13, 8
      beq   x13, x12, Loop
```

a) Assume that branch prediction is used and the branch instruction is predicted wrongly as not taken at the end of the first iteration. Draw the multi-cycle pipeline diagram for the execution of the first two iterations of this loop to find how many cycles are needed to fetch and commit the two iterations.

b) Now assume that this processor has perfect branch prediction with no branch delay. Estimate the number of cycles needed to execute 1,000 iterations of this loop ignoring the time needed to fill the pipeline? (Show your work clearly)

P4. Assume you have a two-way set associative cache with four-word blocks and a total size of 32 words. Assume also that the cache is initially empty and uses true LRU replacement policy. For the following sequence of word-address references (not byte addresses), trace by completing the table below the behavior of the cache. For each reference, identify: the binary word address, the tag, the index, the word offset, whether the reference is a hit or a miss (compulsory, conflict or capacity), and which tags are in each way of the cache after the reference has been handled.

0x03, 0xb4, 0x2b, 0x02, 0xbe, 0x58, 0xbf, 0x0e, 0x1f, 0xbc

Word Address	Binary Address	Tag	Index	Word Offset	Hit/Miss	Miss Type	Way 0	Way 1
0x03	00000011	0	0	3	M	Comp.	**T(0)=0** T(1)=- T(2)=- T(3)=-	T(0)=- T(1)=- T(2)=- T(3)=-
0xb4								
0x2b								
0x02								
0xbe								
0x58								
0xbf								
0x0e								
0x1f								
0xbc								

* Bold indicates most recently accessed way.

P5. Draw a diagram that shows the TLB and cache interaction of a system with the following specifications: 32-bit virtual and physical addresses, 4-KB pages, 8-entry fully-associative TLB, and 4-way associative, physically-tagged, 16-Kbyte cache of 64-byte blocks. You must show the widths of all busses and the TLB and the cache hit circuits.

P6. Dependability

a) The following figure shows the parity bits, data bits, and field coverage in a Hamming ECC code for eight data bits. Assume that you have a memory module that uses this ECC code and that the binary sequence **110001000101** is read from the memory and it has a single bit error. What are the original eight data bits?

Bit position		1	2	3	4	5	6	7	8	9	10	11	12
Encoded data bits		p1	p2	d1	p4	d2	d3	d4	p8	d5	d6	d7	d8
Parity bit coverage	p1	X		X		X		X		X		X	
	p2		X	X			X	X			X	X	
	p4				X	X	X	X					X
	p8								X	X	X	X	X

b) Who uses RAID 51 and why?