0907432 Computer Design (Fall 2019)

Quiz 2

الاسم: رقم التسجيل: رقم الشعبة: 1

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Instructions: Time **20** minutes. Open book and notes exam. No electronics. Please answer all problems in the space provided and limit your answer to the space provided. **No questions are allowed**.

<Good Luck>

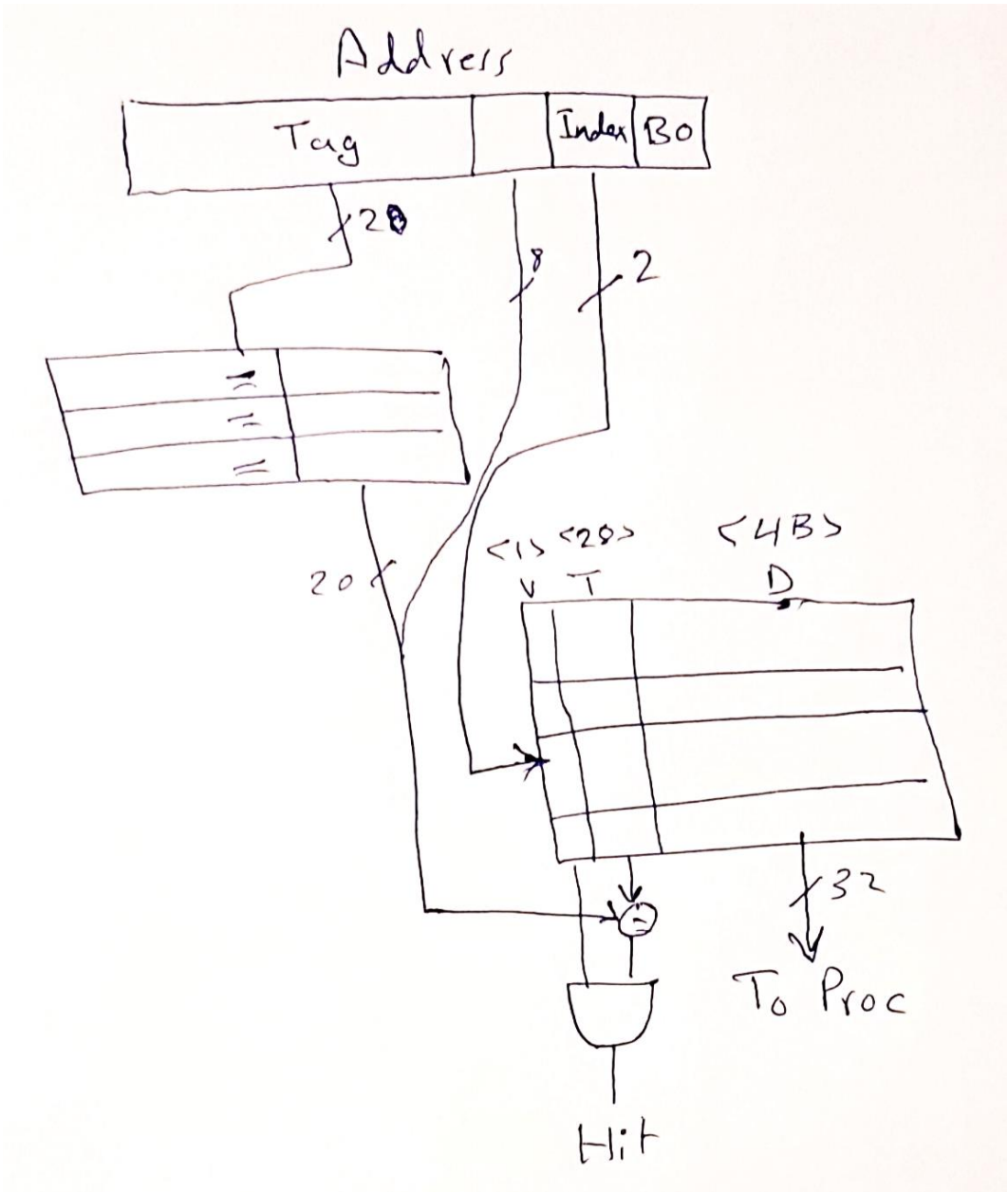
P1. Draw a diagram that shows the TLB and cache interaction of a system with the following specifications: 32-bit virtual and physical addresses, 4-KB pages, 3-entry fully-associative TLB, and direct-mapped, physically-tagged, 16-byte cache of 4-byte blocks. You must show the widths of all busses and the TLB and the cache hit circuits.

The solution is:

<block offset> = lg_2 4 = 2 bits

<index> = lg_2 4 = 2 bits

<tag> = 32 – 2 – 2 = 28 bits



P2. The following figure shows the parity bits, data bits, and field coverage in a Hamming ECC code for eight data bits. Assume that you have a memory module that uses this ECC code and that the binary sequence **110001000101** is read from the memory and it has a single bit error. What are the original eight data bits?

Bit position		1	2	3	4	5	6	7	8	9	10	11	12
Encoded data bits		p1	p2	d1	p4	d2	d3	d4	p8	d5	d6	d7	d8
Parity bit coverage	p1	X		X		X		X		X		X	
	p2		X	X			X	X			X	X	
	p4				X	X	X	X					X
	p8								X	X	X	X	X

123456789012
110001000101
ppdpdddpdddd

The data bits are 0010 0100

p1 = xor(1 0 0 0 0 0) = 1
p2 = xor(1 0 1 0 1 0) = 1
p4 = xor(0 0 1 0 1) = 0
p8 = xor(0 0 1 0 1) = 0

The error code is 0011 -> error in bit 3.

So the data is 1010 0101