# 0907432 Computer Design (Fall 2019)
## Midterm Exam

الاسم: رقم التسجيل: الرقم التسلسلي:

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**Instructions**: Time **60** minutes. Open book and notes exam. No electronics. Please answer all problems in the space provided and limit your answer to the space provided. There are six problems and each problem is for 5 marks. **No questions are allowed**.

*<Good Luck>*

**P1.** Suppose we have two implementations of the same instruction set architecture. Computer A has a clock rate of 2.0 GHz and a CPI of 2.0 for some program, and Computer B has a clock rate of 2.4 GHz and a CPI of 1.2 for the same program. Which computer is faster for this program and by how much?

**Solution:**

**CPU time = IC × CPI / f**

**Assume the instruction count is I**

**CPU time$_A$ = I × 2.0 / 2.0 GHz = I ns**

**CPU time$_B$ = I × 1.2 / 2.4 GHz = I/2 ns**

**B is faster by I / (I/2) = 2 times**

**P2.** For the RISC-V code shown below, perform code scheduling and register renaming to avoid stalls on the five-stage pipeline and to eliminate name and output dependencies. Assume that the branch is resolved in the decode stage. Use registers x0 through x31.

| Original Code | Scheduled Code |
|---|---|
| `add x1, x2, x3`<br>`beq x1, x0, L`<br>`ld x1, 0(x5)`<br>`add x4, x1, x6`<br>`beq x0, x0, S`<br>`L:`<br>`ld x1, 0(x5)`<br>`sub x4, x1, x6`<br>`S:` | **Solution**<br>`add x1, x2, x3`<br>`ld x10, 0(x5)`<br>`beq x1, x0, L`<br>`add x4, x10, x6`<br>`beq x0, x0, S`<br>`L:`<br>`sub x4, x10, x6`<br>`S:` |

**P3.** Consider the following loop.

```
L: ld   x10, 0(x13)
   ld   x11, 8(x13)
   add  x12, x10, x11
   subi x13, x13, 16
   bnez x12, L
```

Assume that perfect branch prediction is used (no stalls due to control hazards), that the pipeline has full forwarding support, and that branches are resolved in the EX (as opposed to the ID) stage. Show a pipeline execution diagram for the first two iterations of this loop.

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| L: ld x10, 0(x13) | F | D | E | M | W | | | | | | | | | | | | | |
| ld x11, 8(x13) | | F | D | E | M | W | | | | | | | | | | | | |
| add x12, x10, x11 | | | F | D | D | E | M | W | | | | | | | | | | |
| subi x13, x13, 16 | | | | F | F | D | E | M | W | | | | | | | | | |
| bnez x12, LOOP | | | | | | F | D | E | M | W | | | | | | | | |
| L: ld x10, 0(x13) | | | | | | | F | D | E | M | W | | | | | | | |
| ld x11, 8(x13) | | | | | | | | F | D | E | M | W | | | | | | |
| add x12, x10, x11 | | | | | | | | | F | D | D | E | M | W | | | | |
| subi x13, x13, 16 | | | | | | | | | | F | F | D | E | M | W | | | |
| bnez x12, LOOP | | | | | | | | | | | | F | D | E | M | W | | |
| | | | | | | | | | | | | | | | | | | |

**P4.** Assume that the following code sequence is executed by a speculative pipelined processor of degree 3. This processor uses reservation stations, common data buses, and reorder buffer. The fetch stage takes one cycle and the issue stage takes one cycle. The integer/branch latency is 1 cycle and the load latency is 2 cycles (1 cycle for address calculation and 1 cycle for data memory access). The processor has two address calculation units, two memory access units, one integer ALU unit, and one branch unit. Using the multi-cycle pipeline diagram below, specify the execution of these instructions in this processor pipeline.

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| ld x2,0(x1) | F | I | A | M | W | C | | | | | | | | | |
| ld x3,8(x1) | F | I | A | M | W | C | | | | | | | | | |
| ld x4,16(x1) | F | I | | A | M | W | C | | | | | | | | |
| add x4,x4,x3 | | F | I | | | | E | W | C | | | | | | |
| sd x4,0(x10) | | F | I | A | | | | | C | | | | | | |
| sd x6,0(x4) | | F | I | | | | | | A | C | | | | | |

**P5.** Schedule the following code sequence in the table below for a static multiple issue processor similar to the one described in the class but is four-issue wide instead of two. Assume that the issue packet can have one ALU instruction, one branch instruction, and two memory instructions as shown in the table below. Note that you need to perform register renaming in order to have an efficient schedule.

```
Loop: ld   x1, 0(x2)
      add  x3, x3, x1

      ld   x1, -8(x2)
      add  x3, x3, x1

      ld   x1, -16(x2)
      add  x3, x3, x1

      addi x2, x2, -24
      bne  x2, x0, Loop
```

| Packet | ALU instruction | Branch instruction | Memory instruction | Memory instruction |
|---|---|---|---|---|
| 1 | | | **ld x1, 0(x2)** | **ld x11, -8(x2)** |
| 2 | **addi x2,x2,-24** | | **ld x12, -16(x2)** | |
| 3 | **add x3,x3,x1** | | | |
| 4 | **add x3,x3,x11** | | | |
| 5 | **add x3,x3,x12** | **bne x2,x0,Loop** | | |
| 6 | | | | |
| 7 | | | | |
| 8 | | | | |

**P6.** The 8-GB DDR3-SDRAM module shown below operates at 800 MHz and has a 64-bit data bus.


a) What is the miss penalty to read a 64-byte block if one cycle is needed to send the request and the data response starts after 20 cycles?

**The solution is:**

**Access time = 1 + 20 + ( 64 / 8 ) / 2**

**= 25 cycles**

b) What is the peak transfer rate of this module?

**The solution is:**

**Peak transfer rate = 8 bytes × 800 MHz × 2**

**= 12,800 MB/s**