0907731 Advanced Computer Architecture (Spring 2018)
Midterm Exam

الاسم: ..... **رقم التسجيل:** ..... **رقم التسلسل:** .....

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Instructions: Time **60** min. Open book and notes exam. No electronics. Please answer all problems in the space provided and limit your answer to the space provided. No questions are allowed. There are six problems and each problem has 5 points.

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P1. A system that features redundancy to improve dependability comprises computing and storage units. The computing part has an active unit and a redundant standby unit. The storage part also has an active unit and a redundant standby unit. If each unit has an MTTF of 1,000 hours and an MTTR of 10 hours, what is the overall system availability?

$MTTF_{computing} = (MTTF^2 / 2) / MTTR = (1000^2 / 2) / 10 = 50{,}000$ hours

$MTTF_{storage} = (MTTF^2 / 2) / MTTR = (1000^2 / 2) / 10 = 50{,}000$ hours

$FIT_{system} = 10^9 / MTTF_{computing} + 10^9 / MTTF_{storage} = 10^9 / 50{,}000 + 10^9 / 50{,}000 = 40{,}000$

$MTTF_{system} = 10^9 / FIT_{system} = 10^9 / 40{,}000 = 25{,}000$ hours

Availability = $MTTF_{system} / (MTTF_{system} + MTTR) = 25{,}000 / (25{,}000 + 10) = 0.9996$

P2. A processor runs on a clock period of 1 ns. Assume that a program has 25% floating-point instructions that take, on average, 4 cycles each and the other 75% instructions take, on average, 1.33 cycle each. Assume that the two design alternates are (1) reducing the CPI of FP instructions to 2 cycles or (2) decrease the clock period to 0.8 ns. Compare these two design alternatives using the processor performance equation and select the best alternative.

Alternative 1:

Time = IC × [0.25 × 2 + 0.75 × 1.33] × 1 = 1.5 IC ns

Alternative 2:

Time = IC × [0.25 × 4 + 0.75 × 1.33] × 0.8 = 1.6 IC ns

Alternative 1 has smaller time, therefore, it is best.

P3. Assume that you have a four-way associative cache that has 64 sets and 128-byte block size.

A) What is the size of this cache?

Cache size = A × No. of sets × Block size = $4 \times 64 \times 128 = 2^2 \times 2^6 \times 2^7 = 2^{15}$ = 32 Kbytes

B) What is the tag size assuming 32-bit address?

<tag> = 32 - <index> - <block offset> = 32 - $\lg_2$ 64 - $\lg_2$ 128 = 32 - 6 - 7 = 19 bits

C) In which cache set the memory address 0x10000A00 (in hexadecimal) will be allocated?

The set is specified by the index bits, which are bits A7 through A12

0 1010 0 = 0x14

P4. Among the following two memory hierarchy design alternatives, which alternative provides better average memory access time?

Feature	Alternative 1	Alternative 2
L1 size and type	32 KB, direct mapped	32 KB, 2-way associative
L1 hit time	1 cycle	2 cycles
L1 miss rate	10%	5%
L2 size and type	256 KB, 4-way associative	256 KB, 2-way associative
L2 hit time	10 cycle	8 cycles
L2 miss rate	2%	3%
Memory access time	100 cycles	100 cycles
Memory miss rate	0	0

Alternative 1:

$AMAT_{L2}$ = 10 + 0.02 × 100 = 12 cycles

AMAT = 1 + 0.1 × 12 = 2.2 cycles

Alternative 2:

$AMAT_{L2}$ = 8 + 0.03 × 100 = 11 cycles

AMAT = 2 + 0.05 × 11 = 2.55 cycles

Alternative 1 has smaller time, therefore, it is best.

P5. An SDRAM DIMM that uses the DDR4-2400 standard runs on a bus clock of 1200 MHz, has 32 GB capacity, and holds 9 SDRAM chips.

A) What is its peak transfer rate?

Peak Transfer Rate = 2 × 1200 × 8 = 19200 MB/s

B) What is the capacity of each SDRAM chip?

Capacity = 32 GB / 8 = 4 GB

C) If the SDRAM chip is 8 bits wide, what is the expected number of address lines that this chip has?

<address> = $\lg_2$ 4G / 2 = 32 / 2 = 16 bits

P6. Assume that the following code sequence is executed by a five-stage pipelined processor that has the latencies shown in the table below. Also assume that branch instructions are resolved in the decode stage. Using the multi-cycle pipeline diagram below, specify the execution of these instructions in this processor pipeline.

Instruction producing result	Instruction using result	Latency in clock cycles
FP ALU op	Another FP ALU op	3
FP ALU op	Store double	2
Load double	FP ALU op	1
Load double	Store double	0

Loop:	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
L.D F0, 0(R1)	F	D	E	M	W												
L.D F2, 0(R2)		F	D	E	M	W											
ADD.D F4, F0, F2			F	D	D	E	E	E	E	M	W						
ADD.D F6, F6, F4				F	F	D	D	D	D	E	E	E	E	M	W		
DADDUI R1, R1, -8						F	F	F	F	D	E	M	W				
DADDUI R2, R2, -8										F	D	E	M	W			
BNE R2, R3, Loop											F	D	D	E	M	W	

<Good Luck>