0907731 Advanced Computer Architecture (Fall 2017)
Midterm Exam

الاسم: ..... رقم التسجيل: ..... رقم التسلسل: .....

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Instructions: Time **75** min. Open book and notes exam. No electronics. Please answer all problems in the space provided and limit your answer to the space provided. No questions are allowed. There are six problems and each problem has 5 points.

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P1. The period from 1986 to 2002 witnessed exponential increase in the processor power consumption.

A) Explain this exponential increase.

The dynamic power equals "½ × Capacitive load × Voltage^2 × Frequency switched". The capacitive load is proportional to the number of transistors. As this number and the frequency increased exponentially during this period, the power consumption increased exponentially.

B) What are the main contemporary techniques used to limit processor power consumption?

Building transistors of lower power consumption, not increasing the frequency, and turning off or stopping the clock off not used components.

P2. A processor runs on a clock rate of 4 GHz. Assume that the program has 50% floating-point instructions that take 4 cycles each and the other instructions take 2 cycle each.

A) What is the CPU time needed to execute a program consisting of 10×10^9 instructions?

Time = $[10\times10^9 \times (0.5 \times 4 + 0.5 \times 2)] / 4\times10^9$

= 2.5 × (2 + 1) = 7.5 seconds

B) Using Amdahl's law, what is the total speed up if the floating-point instructions are sped up by a factor of 2?

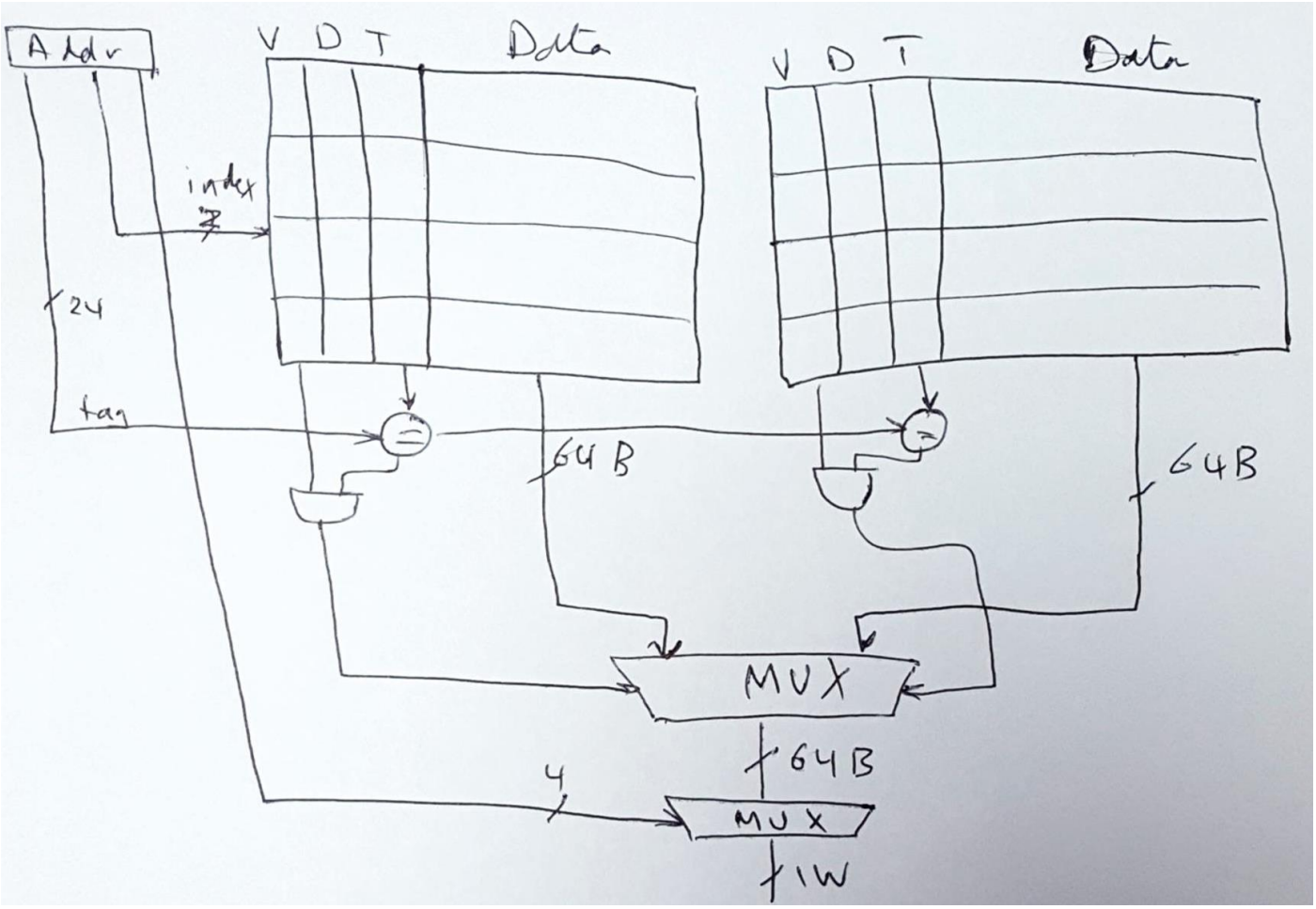
Speedup = 1 / [1/3 + 2/3 / 2] = 1 / [1/3 + 1/3] = 1.5

P3. Draw a two-way associative cache. Assume that the size of this cache is 512 bytes, its block size is 64 bytes, it is a write-back cache, and the address width is 32 bits.

No. of blocks = 512 / 64 = 8 => there are 8/2=4 sets => <index> = 2 bits

<block offset> = $\lg_2$ 64 = 6 bits

<tag> = 32 -6 -2 = 24 bits



P4. What are the effects of the following memory hierarchy optimizations on hit time, miss rate, miss penalty, and bandwidth?

A) Increasing the cache associativity

Hit time ↑, miss rate ↓, miss penalty ↔, bandwidth ↔

B) Using critical word first and early restart

Hit time ↔, miss rate ↔, miss penalty ↓, bandwidth ↑

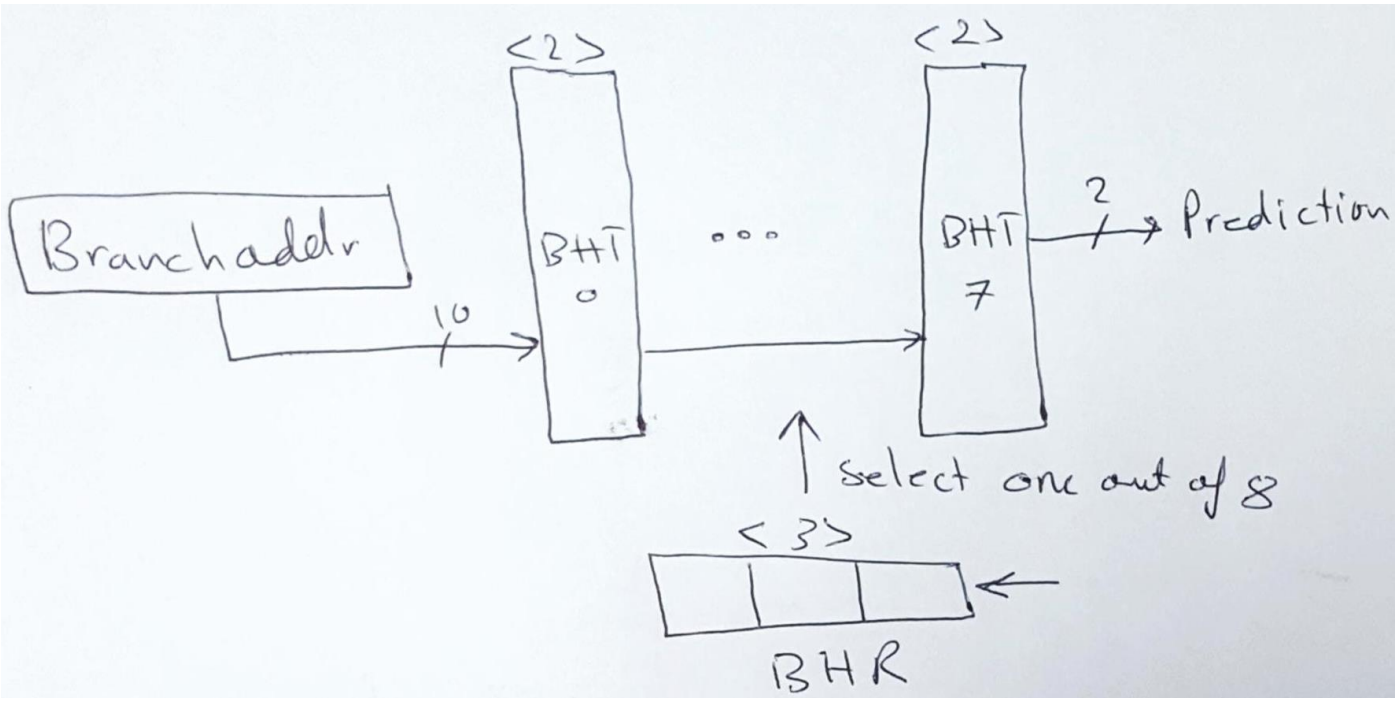
C) Using non-blocking caches

Hit time ↔, miss rate ↔, miss penalty ↓, bandwidth ↑

P5. Draw a 16 Kbit (*m*, *n*) correlating branch predictor. Assume that the shift register size *m* = 3 bits and the branch predictors width *n* = 2 bits.

BHT size = 16 Kbit / (8×2) = 1 K entries

There are 2^3 = 8 BHTs, each is 2 bits wide



6. Assume that the following code sequence is executed by a double-issue speculative pipelined processor. This processor uses reservation stations, common data buses, and reorder buffer. The fetch stage takes one cycle and the issue stage takes one cycle. The integer latency is 1 cycle, the load latency is 2 cycles (1 cycle for address calculation and 1 cycle for data memory access), and the floating-point latency is 2 cycles. The processor has one address calculation unit, one memory access unit, one integer ALU unit, one floating-point unit, and one branch unit. Using the multi-cycle pipeline diagram below, specify the execution of these instructions in this processor pipeline.

Loop:	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
`l.d f0, 0(r1)`	**F**	**I**	**A**	**M**	**W**	**C**									
`l.d f2, 0(r2)`	**F**	**I**		**A**	**M**	**W**	**C**								
`add.d f4, f0, f2`		**F**	**I**				**E**	**E**	**W**	**C**					
`s.d f4, 0(r3)`		**F**	**I**		**A**					**C**					
`daddui r1, r1, -8`			**F**	**I**	**E**	**W**					**C**				
`daddui r2, r2, -8`			**F**	**I**		**E**	**W**				**C**				
`bne r2, r3, Loop`				**F**	**I**			**E**	**W**			**C**			

<Good Luck>