CPE731: Advanced Computer Architecture

Course Introduction

Prof. Gheith Abandah
أ.د. غيث علي عبندة

Outline

- Course Information
- Textbook and References
- Course Outline
- Grading
- Policies
- Important Dates

Course Information

- Instructor: **Prof. Gheith Abandah**
- Email: **abandah@ju.edu.jo**
- Office: **CPE 406**
- Home page:
  http://www.abandah.com/gheith
- Facebook group:

https://www.facebook.com/groups/1439049336332310/

- Prerequisites: **None**
- Office hours: **Mon through Thu, 11:00 – 12:00**

Textbook and References

- **Hennessy and Patterson. Computer Architecture: A Quantitative Approach, 6th ed., Morgan Kaufmann, 2017.**
- Course slides at: http://www.abandah.com/gheith/?page_id=2071
- References:
  - Patterson and Hennessy. Computer Organization & Design: The Hardware/Software Interface, RISC-V ed., Morgan Kaufmann, 2018.
  - J. P. Shen and M. H. Lipasti. Modern Processor Design: Fundamentals of Superscalar Processors, Mc Graw Hill, 2005.
  - D. Culler and J.P. Singh with A. Gupta. Parallel Computer Architecture: A Hardware/Software Approach, Morgan Kaufmann, 1998.
  - J. Hayes. Computer Architecture and Organization, 3rd ed., McGraw-Hill, 1998.
  - Readings in Computer Architecture, Mark Hill (Editor), Norman Jouppi (Editor), Gurindar Sohi (Editor), Morgan Kaufmann Publishing Co., Menlo Park, CA. 1999.

Selected Papers

- Trace Cache: A Low Latency Approach to High Bandwidth Instruction Fetching by E. Rotenberg, S. Bennett, and J.E. Smith, Proceedings of the 29th Annual International Symposium on Microarchitecture, November 1996. First paper on trace caches.
- Combining Branch Predictors, S. McFarling, WRL Technical Note TN-36, June 1993. Proposes the gshare branch predictor, covers a few others. See also the paper by Yeh and Patt (below).
- Alternative Implementations of Two-Level Adaptive Branch Prediction by T.-Y. Yeh and Y. N. Patt. Proceedings of the 19th Annual International Symposium on Computer Architecture, June 1992, pp. 124-134. The classic reference on two-level branch prediction.
- Checkpoint processing and recovery: Towards scalable large instruction window processors. By H. Akkary, R. Rajwar, and S. T. Srinivasan. In MICRO 36, December 2003. Reordering without the reorder buffer.
- Implementation of precise interrupts in pipelined processors by J. E. Smith and A. R. Pleszkun. Proceedings of the 12th Annual International Symposium on Computer Architecture, June 1985, pp. 36-44. The original paper on reorder buffers and their alternatives.

Selected Papers – cont.

- The Mips R10000 superscalar microprocessor by K. C. Yeager, IEEE Micro, April 1996. One of the first out-of-order microprocessors. Uses a merged physical register file (unlike the P6).
- The Alpha 21264 microprocessor by R. E. Kessler, IEEE Micro, Mar/Apr 1999. Another out-of-order microprocessor that also uses a merged physical register file. The 21264 was easily the fastest processor available when it came out. The "dual cluster" design that uses two copies of the register file to reduce the complexity and latency of the bypass network is particularly interesting. This paper also has a substantial discussion of the 21264 tournament branch predictor that's also described in the textbook.
- The Microarchitecture of the Pentium® 4 Processor by Glenn Hinton et al. Intel Technology Journal, Vol. 5 Issue 1 (February 2001). Description of the Pentium 4 microarchitecture by the chief designers, includes some comparisons with P6 and some justification of the deep pipeline/high frequency design goal.

Course Outline

Topic	Week
Fundamentals of Quantitative Design and Analysis	1
Memory Hierarchy Design	2
Instruction-Level Parallelism and Its Exploitation	5
Data-Level Parallelism in Vector, SIMD, and GPU Architectures	8
Multiprocessors Thread-Level Parallelism	10
The Warehouse-Scale Computers	12
Domain Specific Architectures	13
Project Presentations	14

Grading

- **Midterm Exam** **30%**
- **Term Project** **30%**
  - The student researches an active research topic in computer architecture.
  - Teams: 1 student each
  - More info later
- **Final Exam** **40%**

Policies

- Attendance is required
- All submitted work must be yours
- Cheating will not be tolerated
- Open-book exams
- Join the facebook group
- Check program announcements at: http://www.facebook.com/pages/Master-in-Computer-Engineering-and-Networks-in-the-University-of-Jordan/257067841079897

Important Dates

Wed 23 Jan, 2019	First Lecture
Wed 20 Mar, 2019	Midterm Exam
Wed 27 Mar, 2019	Term project proposal is due
Wed 24 Apr, 2019	Term project report is due and start of project demonstrations
Wed 24 Apr, 2019	Last Lecture
May 5 – 13, 2019	Final Exam Period