0907432 Computer Design (Fall 2017)
Quiz 1

الاسم: الرقم التسلسلي: رقم الشعبة: 1

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Instructions: Time **30** minutes. Open book and notes exam. No electronics. Please answer all problems in the space provided and limit your answer to the space provided. **No questions are allowed**.

<Good Luck>

Q1. Assume that the 5-stage pipelined processor studied in the class resolves branch instructions in the decode stage and solves data hazards through forwarding and stalls. Use the pipeline diagram below to show how this processor executes the instructions shown below. Assume that the branch is taken. And how many cycles are needed to fetch and complete the execution of these four instructions? ___10__

[5 marks]

Address	Instruction	1	2	3	4	5	6	7	8	9	10	11	12
00000100	lw $1, 4($2)	F	D	E	M	W							
00000104	bne $1, $0, 1		F	D	D	D	E	M	W				
00000108	sw $0, 4($2)			F	F	F	n	n	n	n			
0000010C	sub $3, $4, $5						F	D	E	M	W		

Q2. For the processor described above, draw the block diagram of this processor showing the blocks and paths needed to solve the data hazard for the shown branch instruction using forwarding and stalls.
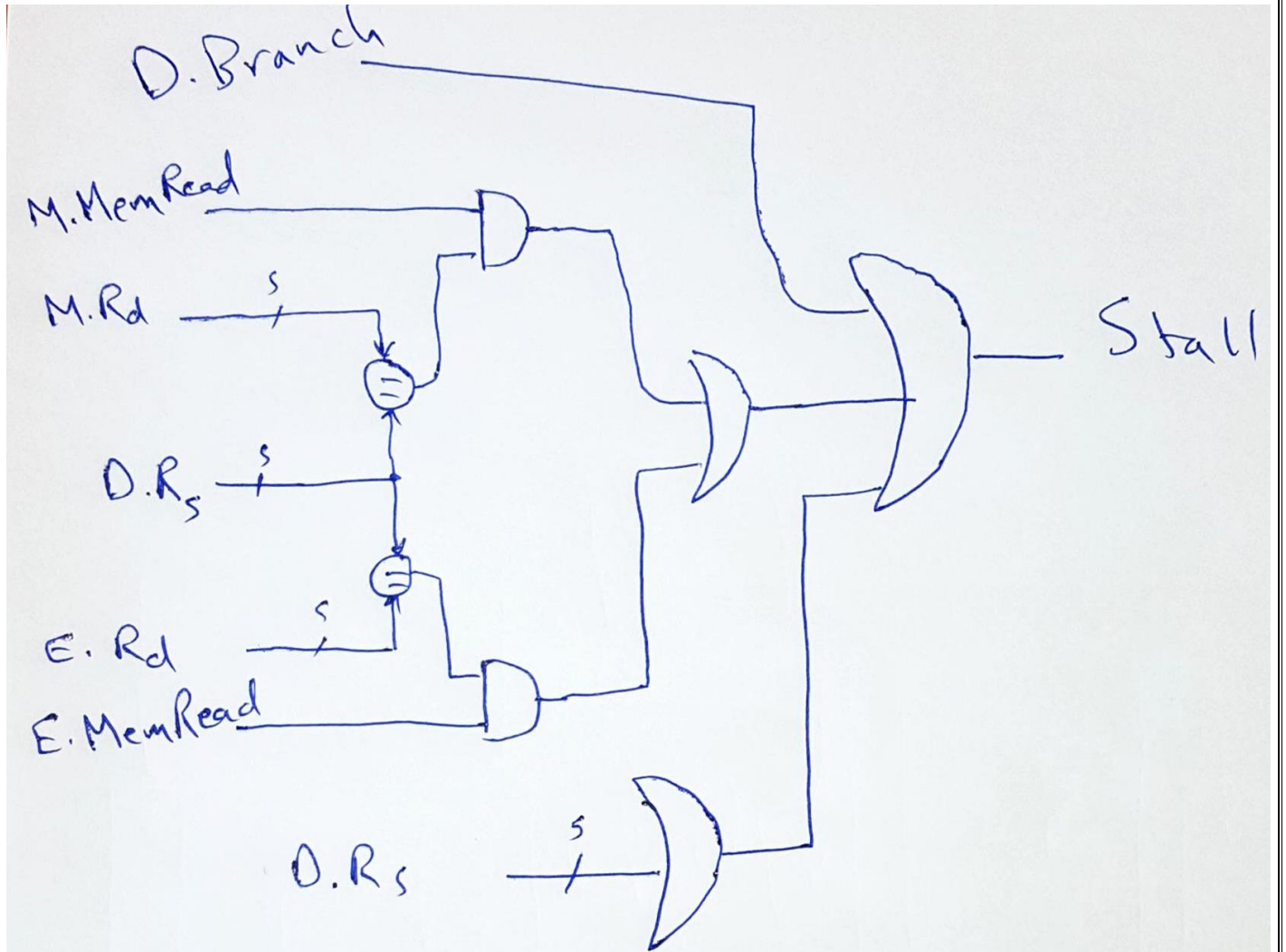
[5 marks]
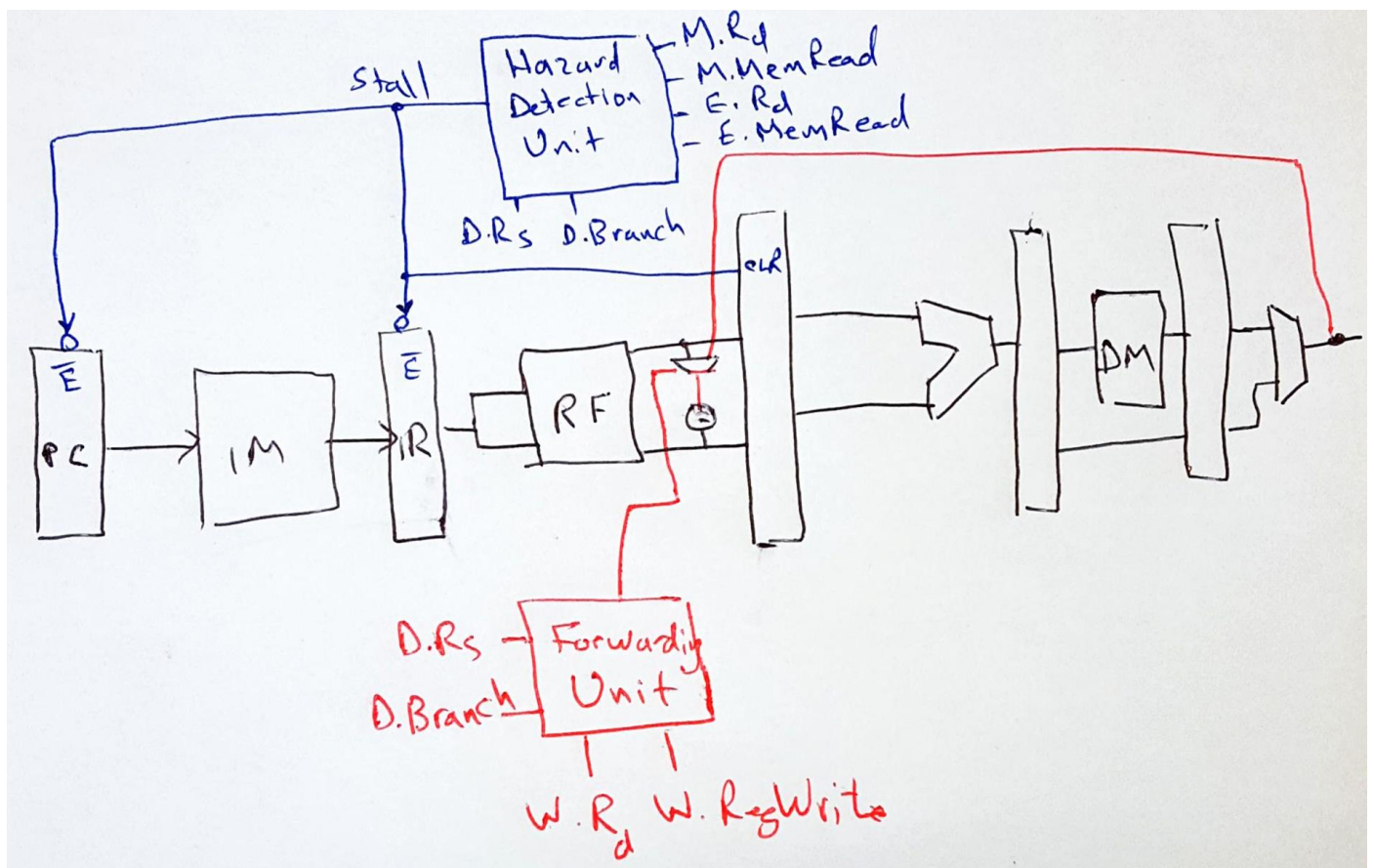
Note that the circuit in red is only needed when the register file does not forward written data to the output in one cycle.

Q3. For the processor described above, draw the circuit needed in the hazard detection unit to detect the data hazard in the shown branch instruction. Design this circuit using basic logic gates.

[5 marks]

D. Branch

M. MemRead

M. Rd

D. R$_s$

E. Rd

E. MemRead

D. R$_s$

Stall

Comparator Circuit

a$_0$
b$_0$

:
:

a$_4$
b$_4$

Equal