

رقم الشعبة: 1

الرقم التسلسلي:

الاسم:

**Instructions:** Time **50** minutes. Open book and notes exam. No electronics. Please answer all problems in the space provided and limit your answer to the space provided. There are six problems and each problem is for 5 marks. **No questions are allowed.**

&lt;Good Luck&gt;

**P1.** For the following performance results of two computers on three benchmarks, find the geometric mean of the relative performance of Computer A to Computer B.

Benchmark	Computer A	Computer B (Reference)	Relative Performance
I	2,000 tps	2,000 tps	1
II	4,000 tps	2,000 tps	2
III	8,000 tps	2,000 tps	4

$$\text{Geometric Mean} = \sqrt[3]{1 \times 2 \times 4} = \sqrt[3]{8} = 2$$

**P2.** According to the latest revisions of Moore's law, the exponential growth of the number of transistors in one dense integrated circuit (IC) is around 30% per year. If the current number of transistors in a dense IC is  $10 \times 10^9$  transistors now, what is the expected number of transistors after two years?

$$\text{Number of transistors} = 10 \times 10^9 \times (1.30)^2$$

$$\text{Number of transistors} = 1.69 \times 10 \times 10^9 = 16.9 \times 10^9$$

**P3.** Perform code scheduling for the following instructions to reduce stalls on a five-stage pipelined processor that resolves branch instructions in the decode stage.

Original Code	Scheduled Code
<pre> lw    r1,0(r2) addi  r3,r3,4 beq   r3,r4,L1 sw    r1,0(r5) L1: </pre>	<pre> addi  r3,r3,4 lw    r1,0(r2) beq   r3,r4,L1 sw    r1,0(r5) L1: </pre>

**P4.** Assume that the following MIPS instructions are executed on a processor that has a branch prediction unit that uses a 1-bit branch history table. Also assume that the BHT is initialized to zeros and the initial prediction is not taken.

```

addi    R1, R0, #0
addi    R2, R0, #16
Loop:  lw    R3, 0(R1)
      add   R4, R4, R3
      addi  R1, R1, #4
      bne  R1, R2, Loop

```

Note that the branch instruction in these instructions is executed four times. Complete the following table to specify for every round of execution of this branch instruction its prediction, actual direction, and whether the prediction is correct or not.

Round	Branch Prediction	Actual Branch Direction	Correct Prediction (Yes or No)?
1	NT	T	No
2	T	T	Yes
3	T	T	Yes
4	T	NT	No

**P5.** Assume that the following code sequence is executed by a triple-issue speculative pipelined processor. This processor uses reservation stations, common data buses, and reorder buffer. The fetch stage takes one cycle and the issue stage takes one cycle. The integer latency is 1 cycle and the load latency is 3 cycles (1 cycle for address calculation and 2 cycles for data memory access). The processor has one address calculation unit, one memory access unit, one integer ALU unit, and one branch unit. Using the multi-cycle pipeline diagram below, specify the execution of these instructions in this processor pipeline.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
lw r2,0(r1)	F	I	A	M	M	W	C								
lw r3,0(r2)	F	I					A	M	M	W	C				
add r5,r3,r4	F	I									E	W	C		
sub r6,r7,r8		F	I	E	W								C		

**P6.** Assume that you have a dual inline memory module (DIMM) that uses DDR3-SDRAM chips operating at 1,000 MHz clock and the DIMM's data bus width is 64 bits. Assume that it takes 28 nsec for the DIMM to start sending the data from the start of the access request. What is the achieved bandwidth in accessing a 64-Byte memory block?

$$\begin{aligned}
 \text{Transfer Time} &= 64 \text{ bytes} \div (64 \text{ bits/transfer} \times (1 \text{ byte}/8 \text{ bits})) \div (2 \text{ transfers/cycle}) \\
 &= 64 \div 8 \div 2 = 4 \text{ cycles} \\
 &= 4 \text{ cycles} \div 1,000 \text{ MHz} \\
 &= 4 \text{ nsec} \\
 \text{Total Time} &= 28 + 4 = 32 \text{ nsec} \\
 \text{Bandwidth} &= 64 \text{ bytes} \div 32 \text{ nsec} \\
 &= 2 \text{ GB/sec}
 \end{aligned}$$