University of Jordan
Computer Engineering Department
Course Outline
Advanced Computer Architecture (0907731)

I. Course Description

Review of computer design principles, processor design, RISC processors, pipelining, and memory hierarchy. Instruction level parallelism (ILP), dynamic scheduling, multiple issue, speculative execution, and branch prediction. Limits on ILP and software approaches to exploit more ILP. VLIW and EPIC approaches. Thread-level parallelism, multiprocessors, chip multiprocessors, and multi-threading. Cache coherence and memory consistency. Advanced memory hierarchy design, cache and memory optimizations, and memory technologies. Advanced topics in storage systems. Designing and evaluating I/O systems.
Prerequisite: None

II. Textbooks and References

1. Hennessy and Patterson. Computer Architecture: A Quantitative Approach, 5th ed., Morgan Kaufmann, 2011. ***Main Textbook***.
2. Patterson and Hennessy. Computer Organization & Design: The Hardware/Software Interface, 5th ed., Morgan Kaufmann, 2013.
3. D. Culler and J.P. Singh with A. Gupta. Parallel Computer Architecture: A Hardware/Software Approach, Morgan Kaufmann, 1998.
4. J. Hayes. Computer Architecture and Organization, 3rd ed., McGraw-Hill, 1998.
5. Readings in Computer Architecture, Mark Hill (Editor), Norman Jouppi (Editor), Gurindar Sohi (Editor), Morgan Kaufmann Publishing Co., Menlo Park, CA. 1999.
6. Trace Cache: A Low Latency Approach to High Bandwidth Instruction Fetching by E. Rotenberg, S. Bennett, and J.E. Smith, Proceedings of the 29th Annual International Symposium on Microarchitecture, November 1996. First paper on trace caches.
7. Combining Branch Predictors, S. McFarling, WRL Technical Note TN-36, June 1993. Proposes the gshare branch predictor, covers a few others. See also the paper by Yeh and Patt (below).
8. Alternative Implementations of Two-Level Adaptive Branch Prediction by T.-Y. Yeh and Y. N. Patt. Proceedings of the 19th Annual International Symposium on Computer Architecture, June 1992, pp. 124-134. The classic reference on two-level branch prediction.
9. Checkpoint processing and recovery: Towards scalable large instruction window processors. By H. Akkary, R. Rajwar, and S. T. Srinivasan. In MICRO 36, December 2003. Reordering without the reorder buffer.
10. Implementation of precise interrupts in pipelined processors by J. E. Smith and A. R. Pleszkun. Proceedings of the 12th Annual International Symposium on Computer Architecture, June 1985, pp. 36-44. The original paper on reorder buffers and their alternatives.
11. The Mips R10000 superscalar microprocessor by K. C. Yeager, IEEE Micro, April 1996. One of the first out-of-order microprocessors. Uses a merged physical register file (unlike the P6).
12. The Alpha 21264 microprocessor by R. E. Kessler, IEEE Micro, Mar/Apr 1999. Another out-of-order microprocessor that also uses a merged physical register file. The 21264 was easily the fastest processor available when it came out. The "dual cluster" design that uses two copies of the register file to reduce the complexity and latency of the bypass network is particularly interesting. This paper also has a substantial discussion of the 21264 tournament branch predictor that's also described in the textbook.

III. Student Materials

Textbook, References, Class Handouts, Web Homepages, PC, and the Internet.

IV. College Facilities

A classroom with whiteboard and projection facilities, library, and computer laboratory.

V. Instructional Methods

1. Lectures
2. Office discussions
3. Projects and presentations by the students
4. Course homepage at http://www.abandah.com/gheith/?page_id=1112
5. Facebook group posts and discussions on https://www.facebook.com/groups/1439049336332310/

VI. Evaluation of Outcomes

1. Mid-Term Exam — 30%
2. Term Project's Report and Presentation — 30%
3. Final Exam — 40%

VII. Class Policies

- Attendance is required
- All submitted work must be yours
- Cheating will not be tolerated
- Open-book exams
- Join the facebook group
- Check program announcements at: http://www.facebook.com/pages/Master-in-Computer-Engineering-and-Networks-in-the-University-of-Jordan/257067841079897

VIII. Course Outline

- Introduction
- Memory Hierarchy Design
- Instruction-Level Parallelism and Its Exploitation

Midterm Exam

- Data-Level Parallelism
- Thread-Level Parallelism
- Warehouse-Scale Computers

Final Exam

IX. Schedule

The following table contains the important dates of this course.

Date	Event
Mon 2 Feb, 2015	Classes Begin
Mar 15 – Apr 2, 2015	Midterm Exam Period
Mon 23 Mar, 2015	Term project proposal is due
Mon 27 Apr, 2015	Term project report is due and start of project demonstrations
Wed 6 May, 2015	Last Lecture
May 13 – 21, 2015	Final Exam Period

X. Sections and Instructors

Sec	Meeting Time	Room	Instructor	Office Hours	e-mail, Homepage
1	Mon & Wed 5:00-6:15	CPE 001	Dr. Gheith Abandah	Sun - Wed 11-12	abandah@ju.edu.jo, http://www.abandah.com/gheith