0907731 Advanced Computer Architecture (Spring 2015)
Midterm Exam

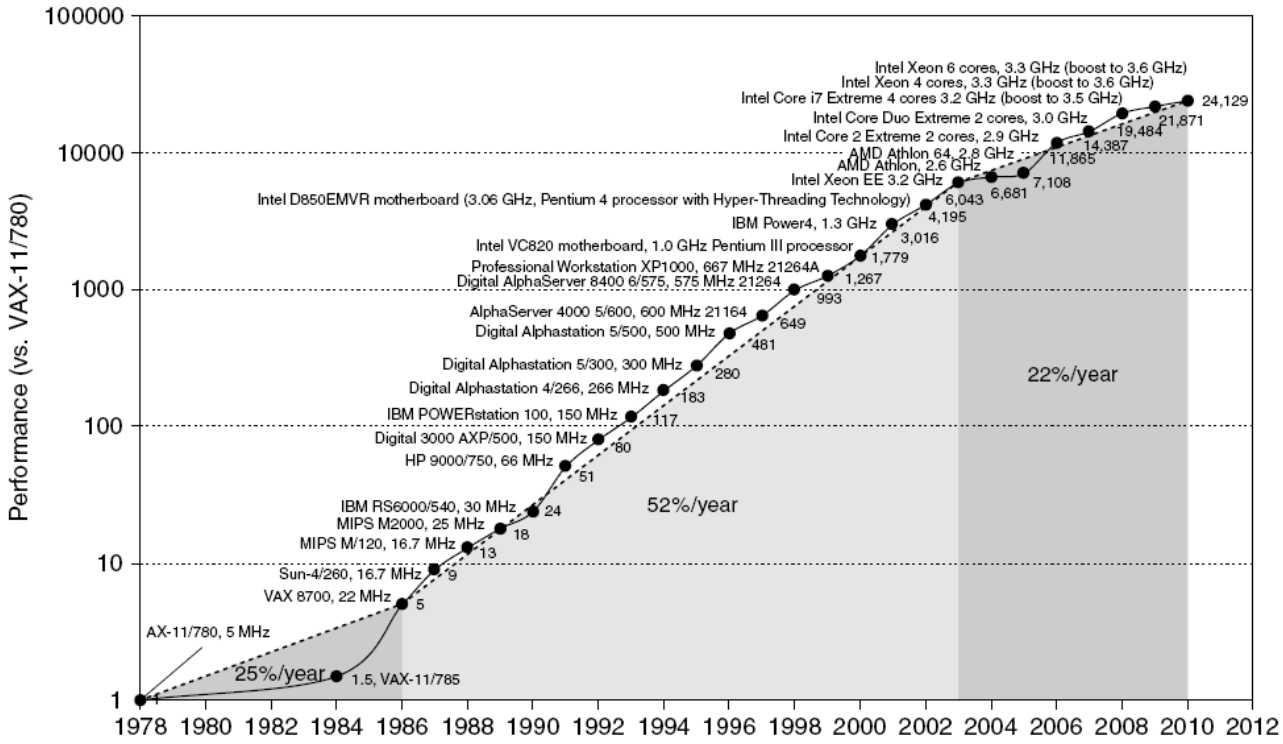
الاسم: ..... رقم التسجيل: ..... رقم التسلسل: .....

==========

Instructions: Time **75** min. Open book and notes exam. No electronics. Please answer all problems in the space provided and limit your answer to the space provided. No questions are allowed. Every question has 5 points.

==========

Q1. The figure below shows the growth in processor performance. The period from 1986 to 2003 has an exponential growth of 52% per year. Give the two main explanations for this growth.



____ **Architectural Innovations** _____

____ **Technological Advancements** _____

Q2. A computer system is made up of the components shown in the following table. What is the availability of this system? _____

Component	Count	MTTF	MTTR
CPU	4	500,000 hours	2 hours
DIMM	6	500,000 hours	2 hours
Disk	8	100,000 hours	2 hours

FIT $= 4 * 10^9 / 500{,}000 + 6 * 10^9 / 500{,}000 + 8 * 10^9 / 100{,}000$

$= 10^3 * (8 + 12 + 80)$

$= 100{,}000$

System MTTF $= 10^9 / 100{,}000 = 10{,}000$ hours

Availability $= 10{,}000 / (10{,}000 + 2) = 0.9998$

Q3. For a two-way associative cache that uses 32-bit address and LRU replacement policy, assume that this cache has 32 blocks and each block is 16 bytes wide. Starting from power on, complete the following table for the hexadecimal byte-addressed cache references shown in the first column.

Address	Block Address	Cache Index	Hit or Miss
00000024	2	2	Compulsory Miss
0000002C	2	2	Hit
00000120	12	2	Compulsory Miss
00000004	0	0	Compulsory Miss
00000028	2	2	Hit
00000058	5	5	Compulsory Miss
0000062C	62	2	Compulsory Miss
00000124	12	2	Conflict Miss

Q4. Assume that you have a simple memory hierarchy consisting of a two-way associative cache and a main memory. Also assume that the cache hit time is two cycles, the miss rate is 2%, and the miss penalty is 100 cycles.

a) What is the average memory access time (AMAT)?

$AMAT_{old}$ = 2 + 0.02 * 100 = 4 cycles

b) What is the AMAT speedup when way prediction is used? Assume that the way prediction accuracy is 90%, the hit time when the prediction is correct is one cycle, and the hit time when the prediction is incorrect is three cycles.

$AMAT_{new}$ = 0.9 * 1 + 0.1 * 3 + 0.02 * 100 = 0.9 + 0.3 + 2 = 3.2 cycles

Speed up = 4 / 3.2 = 1.25

Q5. Complete the following table for the 2-bit branch predictor studied in the class for a branch instruction that is executed five times. Assume that the initial predictor state for this branch is 00 (predict not taken).

Run	Predictor Contents	Branch Prediction	Actual Branch Direction	Prediction Correct (Yes/No)
1	00	**Not Taken**	Taken	**No**
2	**01**	**Not Taken**	Taken	**No**
3	**10**	**Taken**	Taken	**Yes**
4	**11**	**Taken**	Not Taken	**No**
5	**10**	**Taken**	Note Taken	**No**

Q6. Assume that you have a typical 5-stage pipelined processor that uses forwarding and stalls to solve data hazards. After you do code scheduling (modifying and rearrange instructions) for the following code sequence, the minimum number of cycles needed to execute this sequence is: ____**8**_____ cycles

(*You must show your modified code in the right space*)

Original Code Sequence	Rearranged and Modified Code Sequence

L1: lw R5, 0(R1)
add R6, R5, R5
lw R5, 0(R2)
add R7, R5, R5
	L1: lw R5, 0(R1)
	lw R30, 0(R2)
	add R6, R5, R5
	add R7, R30, R30

```
                                1 2 3 4 5 6 7 8
L1:   lw      R5, 0(R1)         F D E M W
      lw      R30, 0(R2)          F D E M W
      add     R6, R5, R5            F D E M W
      add     R7, R30, R30            F D E M W
```

<Good Luck>