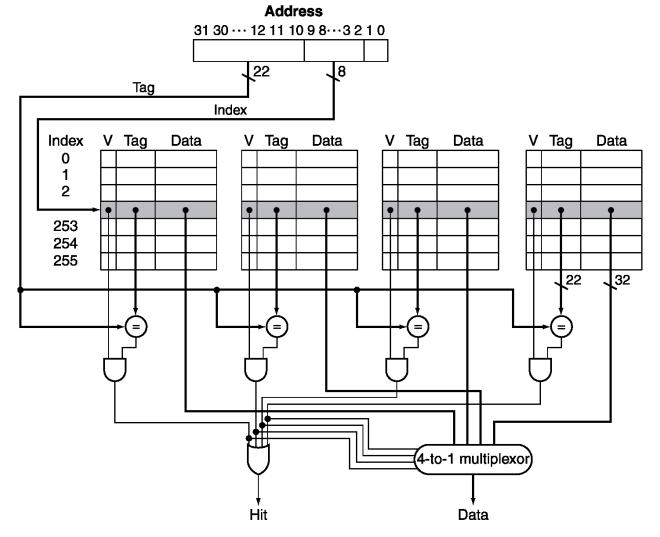
0907432 Computer Design (Summer 2014) <u>Quiz 2</u>

الاسم: الرقم التسلسلي: رقم الشعبة: 1

<u>Instructions</u>: Time 15 minutes. Open book and notes exam. No electronics. Please answer all problems in the space provided and limit your answer to the space provided. No questions are allowed.

<Good Luck>

Q1. Consider the following cache.



Expand the block offset from 2 to lg_2 (128/8) = 4 bits

Shorten the tag from 22 to 20 bits

Add another 4-to-1 multiplexor at the data output controlled by Address Bits 2 and 3

A) How many sets does this cache have?

[1 marks]

256 sets

B) How many blocks does this cache have?

[1 marks]

$4 \times 256 = 1024$ blocks

C) Modify the above diagram such that the block size becomes 128 bits instead of 32 bits.

[3 marks]

Q2. Rewrite the following loop to improve its data locality.

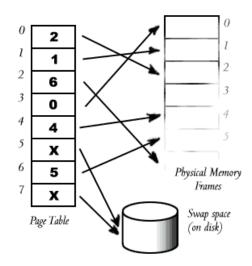
```
[2 marks]
```

```
for (i=0; i<10000; i++) {
  for (j=0; j<10000; j++)
    A[i][j] = A[i][j] * s;
  for (j=0; j<10000; j++)
    B[i][j] = B[i][j] + A[i][j];
}

for (i=0; i<10000; i++) {
  for (j=0; j<10000; j++) {
    A[i][j] = A[i][j] * s;
    B[i][j] = B[i][j] + A[i][j];
  }
}</pre>
```

Q3. Given the following page table and assuming that the page size is 4 KB,

[3 marks]



- A) Does the virtual address 00003ABC₁₆ generate a page fault? _____No____
- B) What is the physical address of the virtual address 00003ABC₁₆? _____00000ABC₁₆