0907432 Computer Design (Summer 2014)

Quiz 1

الاسم: الرقم التسلسلي: رقم الشعبة: 1

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Instructions: Time **15** minutes. Open book and notes exam. No electronics. Please answer all problems in the space provided and limit your answer to the space provided. **No questions are allowed**.

<Good Luck>

Q1. Assume that you have a typical 5-stage pipelined processor that resolves branch instructions in the memory stage. Assume that the CPI of branch instructions is 4 cycles and their instruction frequency is 20%. The rest 80% instructions have an average CPI of 1.2 cycles.

[4 marks]

A) What is the average CPI?

Average CPI = 0.2 × 4 + 0.8 × 1.2
= 0.8 + 0.96
= 1.76 cycles

B) What is the overall speed up when the branches are resolved in the decode stage?

New branch CPI is 2 cycles
New Avg CPI = 0.2 × 2 + 0.8 × 1.2
= 0.4 + 0.96
= 1.36 cycles
Speed up = 1.76 / 1.36 = 1.3

Q2. Assume that you have a typical 5-stage pipelined processor that uses forwarding and stalls to solve data hazards. Assume also that the processor resolves branch instructions in the decode stage. Use the three pipeline diagrams below to find the minimum number of cycles needed by this processor to execute each of the three instruction sequences. Show on the pipeline diagrams any forwarding required using arrows from the producer stage to the consumer stage.

[6 marks]

	1	2	3	4	5	6	7	8	9	10
`lw $t0, 0($s1)`	**F**	**D**	**E**	**M**	**W**					
`sub $t1, $t0, $s2`		**F**	**D**	**D**	**E**	**M**	**W**			

	1	2	3	4	5	6	7	8	9	10
`lw $t0, 0($s1)`	**F**	**D**	**E**	**M**	**W**					
`sw $t0, 0($s2)`		**F**	**D**	**E**	**M**	**W**				

	1	2	3	4	5	6	7	8	9	10
`add $t0, $t1, $s1`	**F**	**D**	**E**	**M**	**W**					
`beq $t2, $t0, Skip`		**F**	**D**	**D**	**E**	**M**	**W**			