0907731 Advanced Computer Architecture (Spring 2014)
Midterm Exam

الاسم: ..... رقم التسجيل: ..... رقم التسلسل: .....

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Instructions: Time **60** min. Open book and notes exam. No electronics. Please answer all problems in the space provided and limit your answer to the space provided. No questions are allowed. Every question has 6 points.

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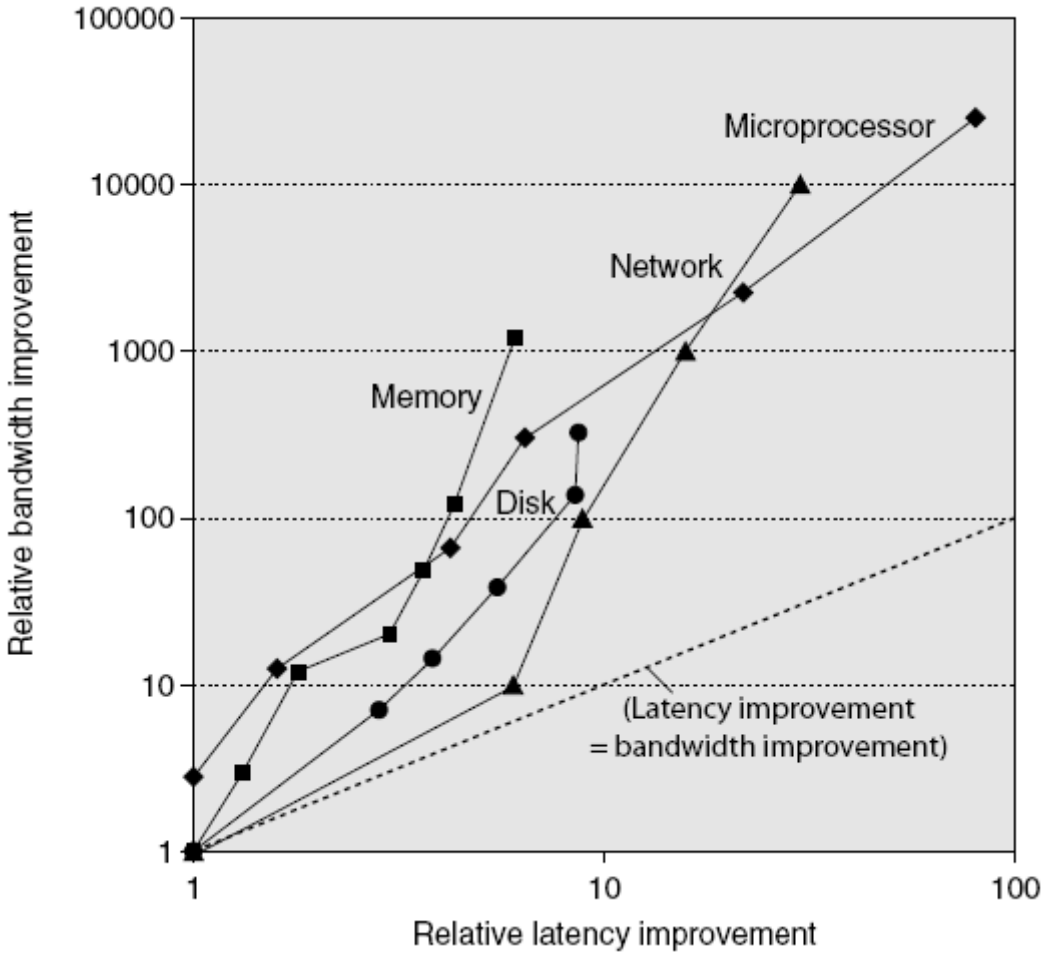
Q1. The following chart tracks relative latency and bandwidth improvements over 20 years. State three main observations based on this chart.



1) **There is an exponential increase in the latency and bandwidth.**

2) **Latency improvements lag bandwidth improvements.**

3) **Best improvements are for microprocessor and network.**

Q2. Describe three techniques to reduce dynamic power and three techniques to reduce static power consumption of modern integrated circuits.

1) **Reduce supply voltage**

2) **Reduce clock rate**

3) **Stop clock for inactive (not used) components**

1) **Reduce supply voltage**

2) **Remove supply off inactive (not used) components**

3) Use smaller circuits with larger transistors

Q3. Assume that you have a simple memory hierarchy consisting of a write-through, write-no-allocate data cache and a main memory. Also assume that 60% of the accesses are load accesses and 40% are store accesses. Assume that the cache hit time is one cycle, the miss rate is 2% for the load operations, the miss penalty is 100 cycles, and the memory write time is 50 cycles.

a) What is the average memory access time (AMAT)?

$AMAT_{old}$ = load time + store time

= 0.6 * (1 + 0.02 * 100) + 0.4 * 50

= 21.8 cycles

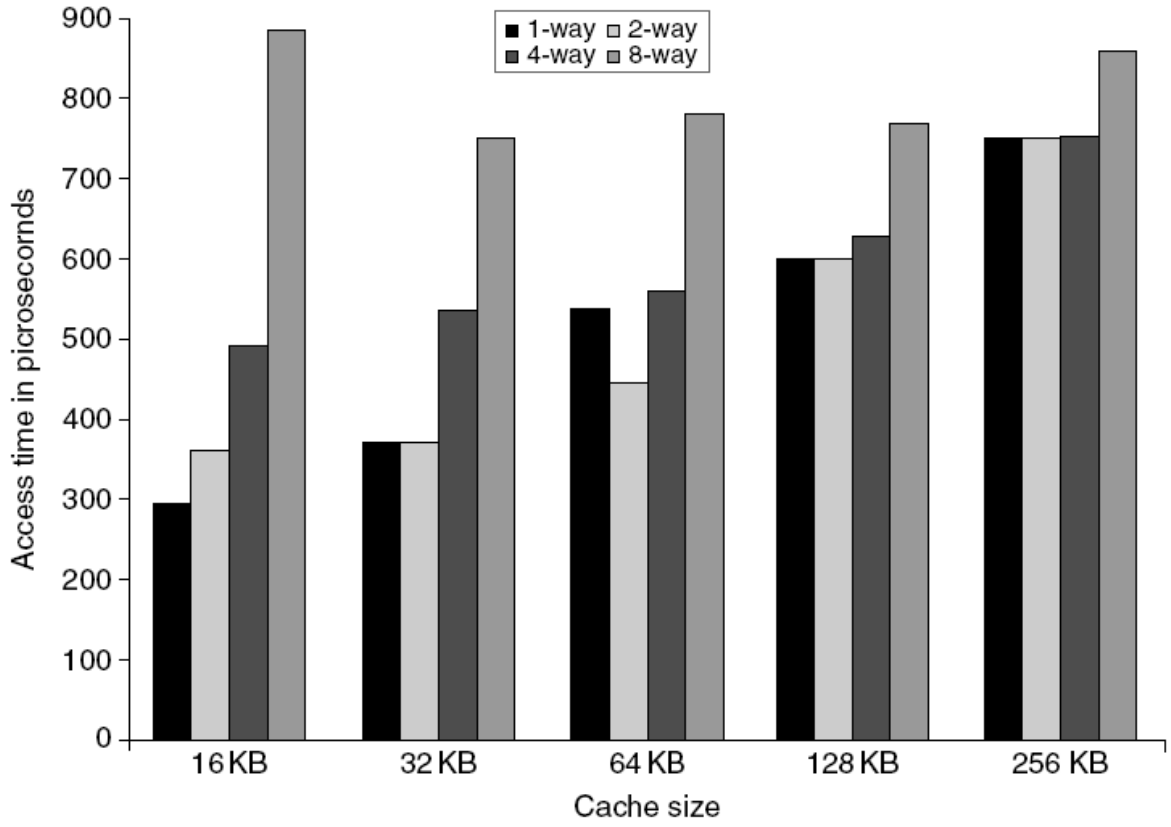
b) What is the AMAT speedup when a write butter is used? Assume that there are no stalls on the write buffer and the miss rate for loads and stores is 2%.

$AMAT_{new}$ = 0.6 * (1 + 0.02 * 100) + 0.4 * 1

= 2.2 cycles

Speed up = 21.8 / 2.2 = 9.9

Q45. Identify and explain the main two trends shown in the following chart for the shown L1 cache size and associativity alternatives.



1. **The access time increases with larger caches due to longer times needed to decode addresses and to propagate signals.**

2. **The access time increases with higher associativity due to the additional time needed to select the hit block.**

Q5. Assume that the following six instructions are executed by a dual-issue processor that uses Tomasolu's algorithm and reorder buffer in executing all instruction types. This processor has sufficient reservation stations for each functional unit. The integer and branch instructions latency is 1 cycle and the memory latency is 2 cycles. The processor has one address calculation units, one memory access unit, one integer ALU unit, one floating-point unit, and one branch unit. Using the pipeline diagram below, find the number of cycles needed to fetch and commit these instructions.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
`Loop:`																	
`lw R3, 0(R0)`	**F**	**I**	**A**	**M**	**W**	**C**											
`lw R1, 0(R3)`	**F**	**I**				**A**	**M**	**W**	**C**								
`addi R1, R1, #1`		**F**	**I**						**E**	**W**	**C**						
`sw R1, 0(R3)`		**F**	**I**				**A**				**C**						
`sub R4, R3, R2`			**F**	**I**		**E**	**W**					**C**					
`bnz R4, Loop`			**F**	**I**				**E**	**W**			**C**					

12 cycles

<Good Luck>