0907432 Computer Design (Fall 2013)

Quiz 2

الاسم: الرقم التسلسلي: رقم الشعبة: 1

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Instructions: Time **15** minutes. Open book and notes exam. No electronics. Please answer all problems in the space provided and limit your answer to the space provided. **No questions are allowed**.

<Good Luck>

Q1. Assume that you have a processor connected to DDR-DRAM memory through a 64-bit bus. Assume also that this bus has a 1-GHz clock and the processor has a cache of 64-byte blocks.

A) What is the peak data transfer rate over this bus?

[2 marks]

Peak transfer rate = 2 transfers/clock * (64/8) bytes/transfer * 1 G clock/sec
= 16 * 10^9 bytes/sec

B) What is the cache read miss penalty if it takes one bus clock cycle to place the request and 50 cycles to access the memory?

[2 marks]

Cycle time = 1 / f = 1 / 1 G Hz = 1 nsec
Miss penalty = request time + access time + transfer time
= 1 nsec + 50 nsed + 64 bytes / (16 * 10^9 bytes/sec)
= 55 nsec

C) What is the AMAT if the hit rate is 99% and the hit time is 1 ns?

[2 marks]

AMAT = hit time + miss rate * miss penalty
= 1 nsec + 0.01 * 55 nsec
= 1.55 nsec

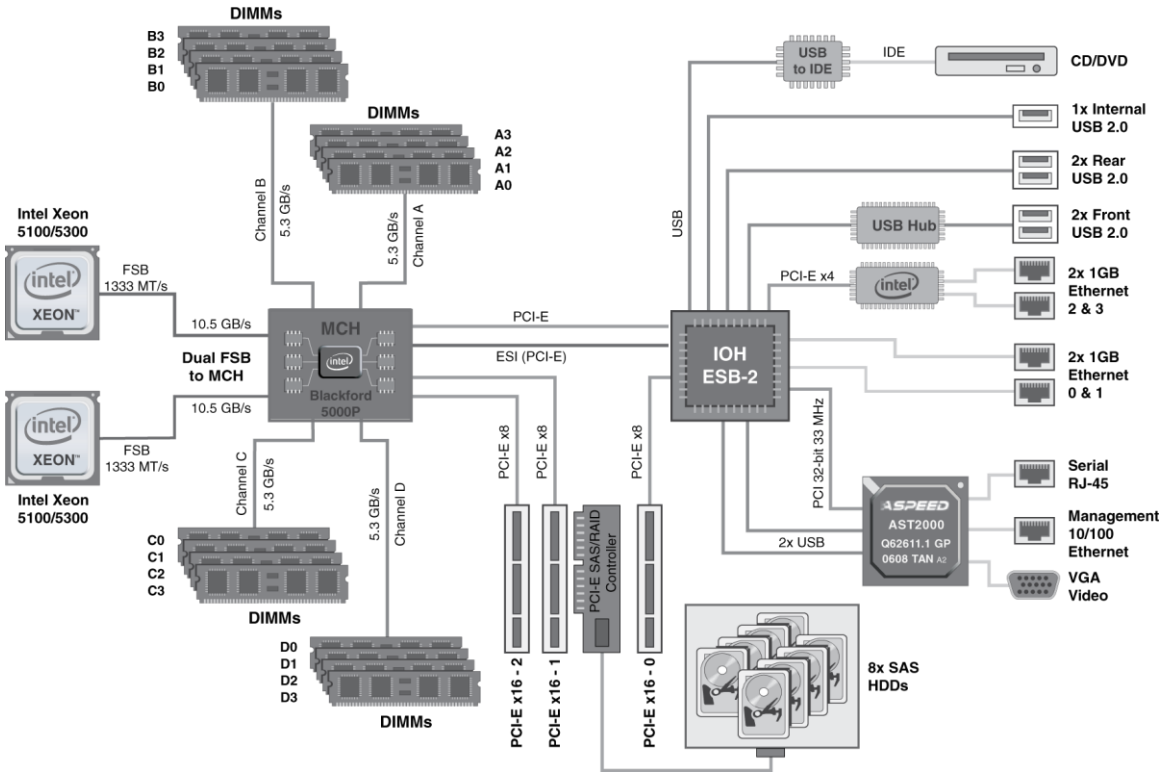
Q2. On a computer that uses 4-KB virtual pages, what is the full page table size of a process assuming that the virtual address is 32 bits and the page table entry is 4 bytes?

[2 marks]

Page table size = size of one entry * number of entries
= 4 bytes * *(2^{32} bytes / 4KB)
= 4 * 2^{32} / 2^{12}
= 4 MB

Q3. Consider the following diagram of the Sun Fire x4150 1U server, what is the peak transfer rate between the hard disk controller and the North Bridge?

[2 marks]



The peak transfer rate between the hard disk controller and the North Bridge

= peak transfer rate on the PCI-E x 8 bus

= number of lanes * lane bandwidth

= 8 lanes * 250MB/s/lane

= 2 GB/s