0907432 Computer Design (Fall 2013) <u>Quiz 1</u>																			
1 :	رقم الشعبة: 1				الرقم التسلسلي:									الاسم:					
Instructions: Time 30 minutes. Open book and notes exam. No electronics. Please answer all problems in the space provided and limit your answer to the space provided. No questions are allowed. <good luck=""></good>																			
<b>Q1.</b> Assume that you have a typical 5-stage pipelined processor that uses forwarding and stalls to solve data hazards. Assume also that the processor resolves branch instructions in the decode stage.														ta					
A) Mark all data dependencies in one iteration of the following MIPS loop. [1.5 marks]													ks]						
Loop: 1	w \$t	0, 0(\$s1	)		#	\$t(	0=a:	rray	v el	eme	nt								
a	ddu \$t	0, \$t0,	\$s2		#	ado	d so	cala	ar i	n \$	s2								
S	w şt	0, 0(\$s1	)		#	sto	ore	res	sult										
a	ddi \$s	li \$ş1, \$s1,-4 # decrement pointer																	
b	ne \$s	1, \$zero	, Loo	p	#	bra	ancl	n \$s	s1!=	=0									
<b>B</b> ) Use the one ite	<ul><li>B) Use the pipeline diagram below to find out how many cycles are needed by this processor to execute one iteration of this loop.</li></ul>														e ksl				
			1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	]	
lw S+	0, 0(ŝ	s1)	F	- D	E	M	W		,		-	10	**	12	10		10	-	
	0 ¢+0	, ć_?		F			<b>F</b>	М	W									-	

			1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
lw	\$t0,	0(\$s1)	F	D	E	Μ	W										
addu	\$t0,	\$t0, \$s2		F	D	D	►	Μ	W								
SW	\$t0,	0(\$s1)			F	F	D	E	M	W							
addi	\$s1,	\$s1,-4					F	D	E	Μ	W						
bne	\$s1,	\$zero, Loop						F	D	D	Е	Μ	W				

Stalls are marked in red and forwardings are marked in blue arrows.

C) In the space below, reorder the instructions of this loop to avoid stall cycles.

[1.5 marks]

```
Loop: 1w $t0, 0($s1)

addi $s1, $s1,-4

addu $t0, $t0, $s2

sw $t0, 4($s1)

bne $s1, $zero, Loop
```

This schedule avoids all stalls and takes 9 cycles.

Q2. A) What is the relation between the die area and the integrated circuit cost?

[2 marks]

Cost  $\alpha$  (die area)<sup>2</sup>

B) Give a justification for this relation.

[2 marks]

- 1) As the area increases, the wafer cost is amortized on fewer ICs.
- 2) As the area increases, the yield decreases because the probability of having a defective die increases.