0907432 Computer Design (Fall 2013)
Midterm Exam

الاسم: الرقم التسلسلي: رقم الشعبة: 1

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Instructions: Time **50** minutes. Open book and notes exam. No electronics. Please answer all problems in the space provided and limit your answer to the space provided. **No questions are allowed**.

<Good Luck>

Q1. Assume that you have a typical 5-stage pipelined processor that uses forwarding and stalls to solve data hazards. Assume also that the processor resolves branch instructions in the decode stage.

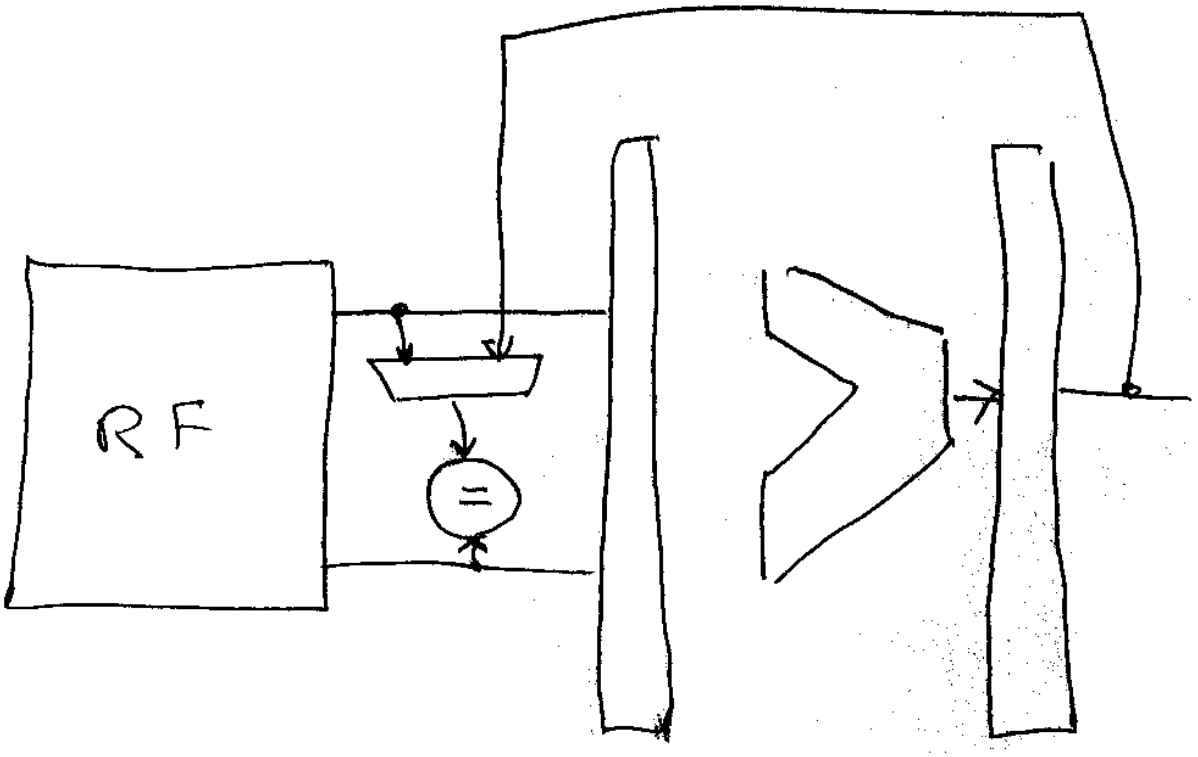
A) Use the pipeline diagram below to find out how many cycles are needed by this processor to execute the shown two MIPS instructions.

[3 marks]

	1	2	3	4	5	6	7	8	9	10
`addi $s1, $s1,-4`	**F**	**D**	**E**	**M**	**W**					
`bne $s1, $zero, -20`		**F**	**D**	**D**	**E**	**M**	**W**			

B) Draw the forwarding circuits needed to resolve the above data hazard. *Don't draw a complete processor; just draw the busses and the logic units required for this forwarding.*

[4 marks]



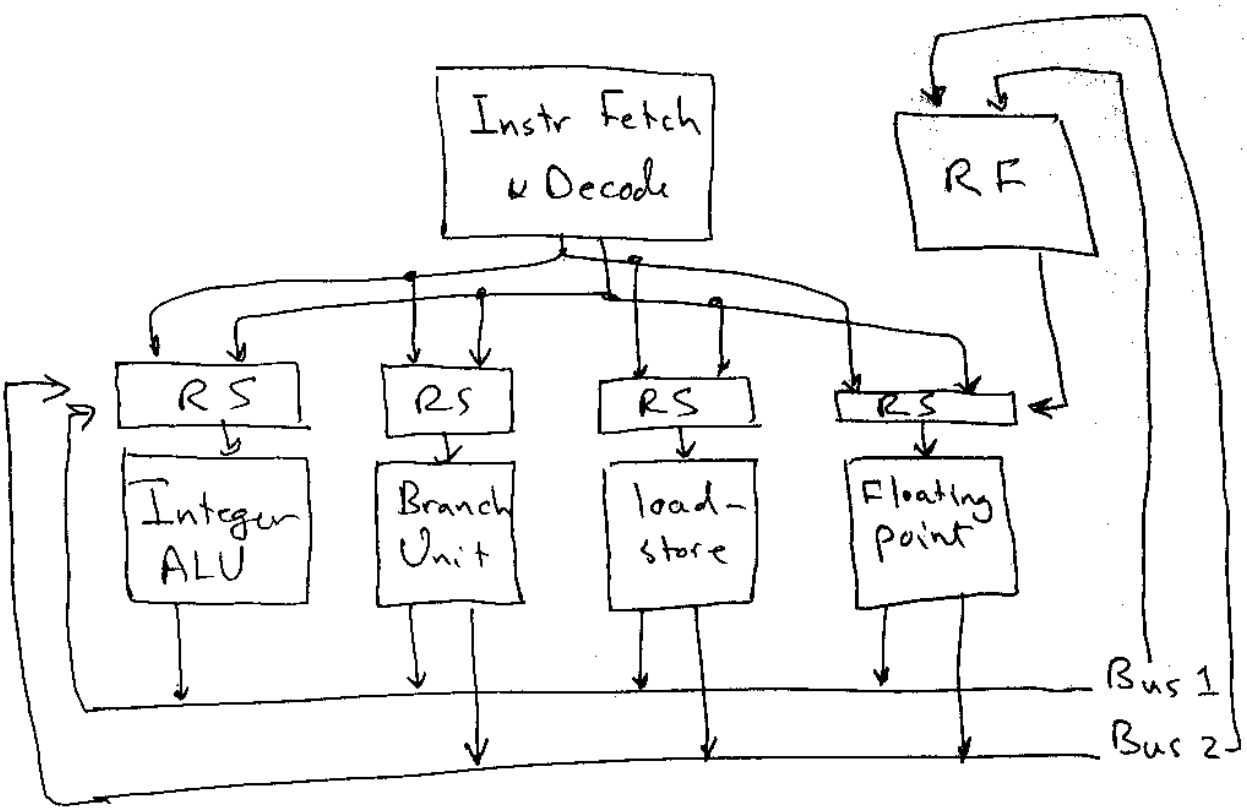
C) What are the conditions to stall the pipeline for this data hazard?

[3 marks]

E.RegWrite ***and*** **E.Rd = D.Rs** ***and*** **D.branch** ***and*** **E.Rd ≠ 0**

Q2. Draw a superscalar processor that can fetch, issue, and write back two instructions per cycle. Assume that this processor supports dynamic scheduling and allows out-of-order execution using reservation stations. Assume also that it has *out-of-order completion* and has the following functional units: integer ALU, branch unit, load-store unit, and floating-point unit. *Show all main busses including the busses from and to the register file*.

[10 marks]



Q3. Assume that you have a two-way associative cache. Also assume that the cache size is 8 KB and the block size is 16 bytes.

A) How many blocks does this cache have?

[2 marks]

8 KB / 16 B = 512 blocks

B) What is the width of the cache index field?

[2 marks]

Sets = 512 blocks / 2 = 256 sets
<index> = $\lg_2$ 256 = 8 bits

C) Complete the following table that shows the byte addresses of six accesses to this cache in hexadecimal. Assume that the cache was empty before these accesses and that the cache uses the LRU replacement. For every byte address, specify its cache index value, whether the access is a hit or miss, and the tag contents of the affected cache block after performing the access.

[6 marks]

Byte Address	Cache Index	Hit or miss	Tag Contents Set 0	Tag Contents Set 1
AABBCC00	**C0**	**Miss**	**AABBC**	
EEDDCC08	**C0**	**Miss**	**AABBC**	**EEDDC**
EEDDCC00	**C0**	**Hit**	**AABBC**	**EEDDC**
AABBCC0C	**C0**	**Hit**	**AABBC**	**EEDDC**
FF00CC04	**C0**	**Miss**	**AABBC**	**FF00C**
EEDDCC00	**C0**	**Miss**	**EEDDC**	**FF00C**