0907432 Computer Design (Summer 2013)

Quiz 2

الاسم: الرقم التسلسلي: رقم الشعبة: 1

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Instructions: Time **20** minutes. Open book and notes exam. No electronics. Please answer all problems in the space provided and limit your answer to the space provided. **No questions are allowed**.

<Good Luck>

Q1. For a two-way associative cache that uses LRU replacement policy, assume that this cache has 8 blocks and each block is 16 bytes wide. Starting from power on, complete the following table for the hexadecimal byte-addressed cache references shown in the first column.

[5 marks]

Address	Block Address	Cache Index	Hit or Miss	Miss Type
00000024	2	2	Miss	Compulsory
0000002C	2	2	Hit	-
000000A0	A	2	Miss	Compulsory
00000004	0	0	Miss	Compulsory
0000002C	2	2	Hit	-
00000059	5	1	Miss	Compulsory
0000006C	6	2	Miss	Compulsory
000000A4	A	2	Miss	Conflict

1 pt

1 pt

1 pt

1 pt

1 pt

Q2. Draw a diagram that shows the TLB and cache interaction of a system with the following specifications: 32-bit virtual address, 4-KB pages, 4-entry fully-associative TLB, and direct-mapped, physically-tagged, 4-KB cache of 4-byte blocks. You must show the widths of all busses and the TLB and the cache hit circuits.

[5 marks]