0907432 Computer Design (Summer 2013)

Midterm Exam

الاسم: الرقم التسلسلي: رقم الشعبة: 1

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Instructions: Time **50** minutes. Open book and notes exam. No electronics. Please answer all problems in the space provided and limit your answer to the space provided. **No questions are allowed**.

<Good Luck>

Q1. Assume that you have a typical 5-stage pipelined processor that uses stalls to solve data hazards. No forwarding paths are available; not even through the register file, i.e., when the register file is updated, the new value will be available for reading in the next cycle. Using multi-cycle pipeline diagrams, find how many cycles are needed to execute the following sequence of MIPS instructions.

[6 marks]

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
`lw R2, 0(R1)`	**F**	**D**	**E**	**M**	**W**										
`add R2, R2, R3`		**F**	**D**	**D**	**D**	**D**	**E**	**M**	**W**						
`sw R2, 0(R1)`			**F**	**F**	**F**	**F**	**D**	**D**	**D**	**D**	**E**	M	W		

Q2. Assume that the following MIPS instructions are executed on a processor that has a branch prediction unit that uses a 2-bit branch history table. Also assume that the BHT is initialized to zeros and the initial prediction is not taken.

[6 marks]

```
      addi    R1, R0, #0
      addi    R2, R0, #16
Loop: lw      R3, 0(R1)
      add     R4, R4, R3
      addi    R1, R1, #4
      bneq    R1, R2, Loop
```

a) How many rounds the branch instruction is executed? __**Four Rounds**_____

b) Complete the following table to specify for every execution of this branch instruction its prediction, actual direction, and whether the prediction is correct or not.

Round	Branch Prediction	Actual Branch Direction	Correct Prediction (Yes or No)?
1	**NT**	**T**	**No**
2	**NT**	**T**	**No**
3	**T**	**T**	**Yes**
4	**T**	**NT**	**No**

Q3. Unroll the following loop three times and schedule it for the two-way static scheduling processor studied in the class.

[6 marks]

```
Loop: lw      R2, 0(R1)
      add     R2, R2, R5
      sw      R2, 0(R1)
      addi    R1, R1, #4
      bneq    R1, R3, Loop
```

```
Loop: lw      R2, 0(R1)
      add     R2, R2, R5
      sw      R2, 0(R1)
      lw      R2, 4(R1)
      add     R2, R2, R5
      sw      R2, 4(R1)
      lw      R2, 8(R1)
      add     R2, R2, R5
      sw      R2, 8(R1)
      addi    R1, R1, #12
      bneq    R1, R3, Loop
```

```
Loop: lw      R2, 0(R1)
      add     R2, R2, R5
      sw      R2, 0(R1)
      lw      R4, 4(R1)
      add     R4, R4, R5
      sw      R4, 4(R1)
      lw      R6, 8(R1)
      add     R6, R6, R5
      sw      R6, 8(R1)
      addi    R1, R1, #12
      bneq    R1, R3, Loop
```

Cycle	ALU/branch	Load/store
1		lw R2, 0(R1)
2	addi R1, R1, #12	lw R4, 4(R1)
3	add R2, R2, R5	lw R6, -4(R1)
4	add R4, R4, R5	sw R2, -12(R1)
5	add R6, R6, R5	sw R4, -8(R1)
6	bneq R1, R3, Loop	sw R6, -4(R1)
7		
8		
9		
10		
11		

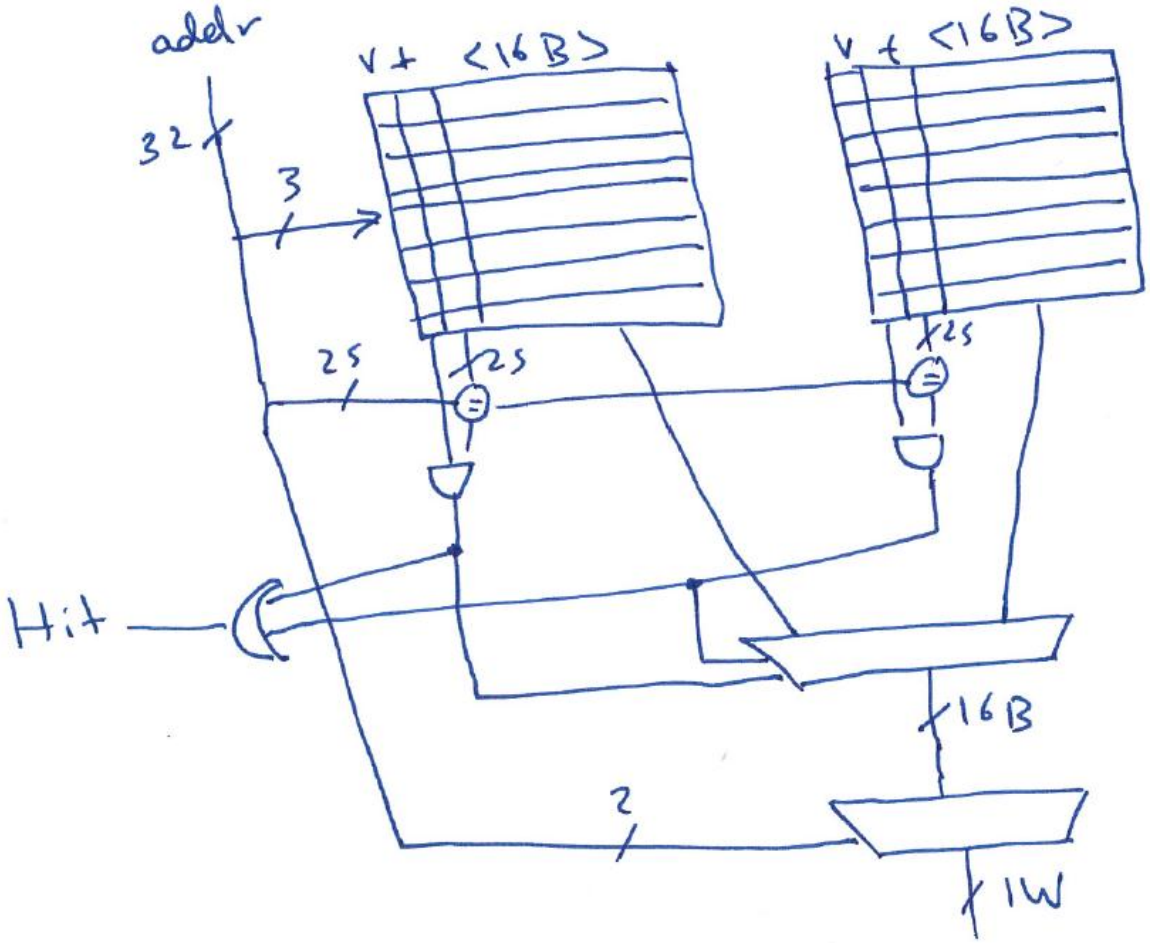
Q4. Design a 256-byte two-way associative cache that has 16-byte blocks. You must specify the width of every memory field and the width of every bus drawn.

[6 marks]

Blocks = 256 / 16 = 16 blocks

Sets = 16 /2 = 8 sets

<tag> = 32 - <index> - <block off.> = 32 – 3 – 4 = 25 bits



Q5. How many bus cycles are needed to read one 64-byte block from a DDR-SDRAM main memory connected with the processor on a 500-MHz bus? Assume that the bus width is 64 bits and the memory access time is 40 ns.

[6 marks]

Cycle time = 1 / 500 MHz = 2 ns

Request time = 1 cycle

Access time = 40 ns / 2 ns/cycle = 20 cycles

Data Transfer Time = 64 bytes/block / 8 bytes/xfer / 2 xfers/cycle = 4 cycles

Total Time = 1 + 20 + 4 = 25 cycles