0907731 Advanced Computer Architecture (Spring 2013)
Midterm Exam

الاسم: ..... رقم التسجيل: ..... رقم التسلسل: .....

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Instructions: Time **60** min. Open book and notes exam. No electronics. Please answer all problems in the space provided and limit your answer to the space provided. No questions are allowed. Every question has 6 points.

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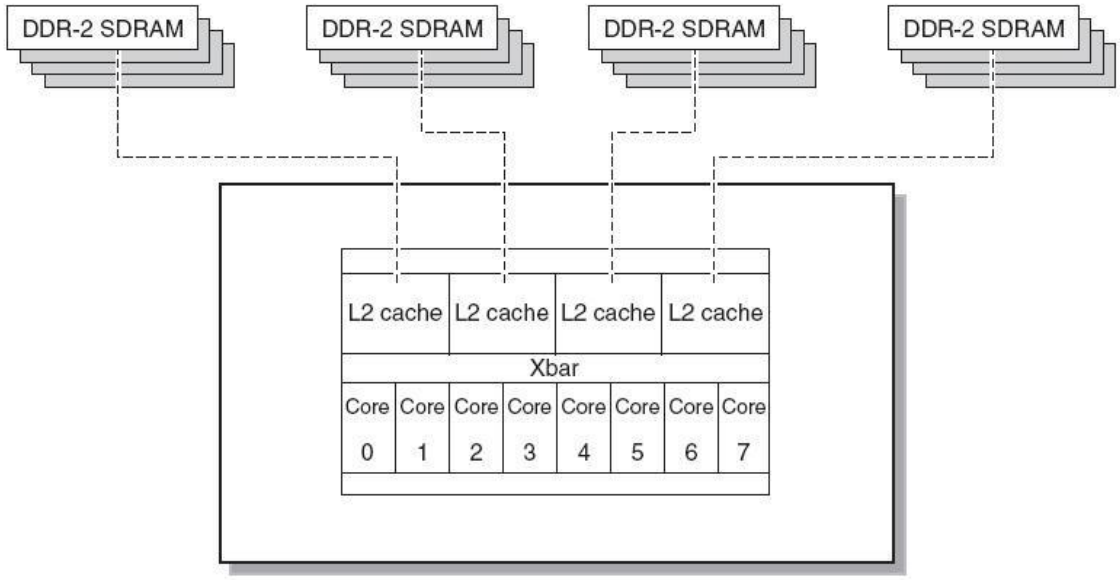
Q1. The figure below shows the block diagram of Sun UltraSPARC T1 processor. Briefly describe this processor.



- **This is an 8-core multi-threaded processor.**
- **Each core has its own L1 caches, but the 8 cores share four banks of L2 caches through the crossbar.**
- **For high memory throughput, each of the four L2 cache banks has one memory port to the DDR2-SDRAM memory. Each cache bank is responsible of caching one fourth of the address space.**

Q2. A program has two phases of execution: It spends 150 seconds in the first phase and 50 seconds in the second phase. You can improve the execution of only one phase by a factor of five. What would be your best overall speedup?

f = 150 / (150 + 50) = 0.75

Speedup = 1 / (1-0.75 + 0.75/5) = 1 / (0.25 + 0.15) = 1 / 0.4 = 2.5

Q3. Assume that you have a variant of the MIPS instruction set architecture that has two operands instead of three. Convert the following C code to this variant of MIPS instructions. Assume that the compiler associates Variables x, y, and z with Register R1, R2, and R3, respectively.

```
if (x == 0)
     x = y + z;
else
     x = x - z;
```

```
     bnez R1, Else
     add  R1, R2
     add  R1, R3
     j    Out
Else:
     sub  R1, R3
Out:
```

Q4. Unroll the following loop twice and schedule it, then find how many cycles are needed to execute one iteration of the unrolled loop. Assume that you have the five-stage pipeline with multi-cycle operations, FP operations take 3 cycles, branch instructions are resolved in the Decode stage, and the processor can write one integer result and one FP result in the Write Back stage every cycle.

```
Loop: l.d       F0, 0(R1)   F D E M W
      l.d       F4, 0(R2)     F D E M W
      mul.d     F0, F0, F4      F D - E E E M W              One stall cycle
      add.d     F2, F2, F0        F - D - - E E E M W        2 stall cycles
      daddi     R2, R2, #-8           F - - D E M W
      daddi     R1, R1, #-8                 F D E M W
      bneq      R1, R3, Loop                  F D - E M W    One stall cycle
```

```
                          1 2 3 4 5 6 7 8 9 0 1 2 3 4 5 6 7 8
Loop: l.d       F0, 0(R1)   F D E M W
      l.d       F4, 0(R2)     F D E M W
      l.d       F6, -8(R1)      F D E M W
      mul.d     F0, F0, F4        F D E E E M W
      l.d       F8, -8(R2)          F D E M W
      daddi     R1, R1, #-16          F D E M W
      mul.d     F6, F6, F8              F D E E E M W
      add.d     F2, F2, F0                F D E E E M W
      daddi     R2, R2, #-16                F D E M W
      add.d     F10, F10, F6                  F D E E E M W
      bneq      R1, Loop                        F D E M W
      add.d     F2, F2, F10
```

Need 11+4 cycles to execute one iteration of the unrolled loop.

Q5. Assume that the following five instructions are executed by a processor that uses Tomasolu's Algorithm in executing all instruction types. This processor has **two** reservation stations for each functional unit. The integer latency is 1 cycle, the memory latency is 2 cycles, and floating-point latency is 2 cycles. The processor has one address calculation unit, one memory access unit, one integer ALU unit, one floating-point unit, and one branch unit. Using pipeline diagram in the space below, find the number of cycles needed to fetch and commit these instructions.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
`lw R1, 0(R2)`	**F**	**I**	**A**	**M**	**W**												
`lw F0, 0(R1)`		**F**	**I**	**-**	**-**	**A**	**M**	**W**									
`add.d F4, F2, F0`			**F**	**I**	**-**	**-**	**-**	**-**	**A_1**	**A_2**	**W**						
`sw F4, 0(R1)`				**F**	**-**	**I**	**A**	**-**	**-**	**-**	**-**	**M**					
`lw R1, 8(R2)`					**F**	**-**	**-**	**-**	**I**	**A**	**M**	**W**					

12 Cycles

<Good Luck>