University of Jordan
Computer Engineering Department
Course Outline
Advanced Computer Architecture (0907731)

I. Course Description

Review of computer design principles, processor design, RISC processors, pipelining, and memory hierarchy. Instruction level parallelism (ILP), dynamic scheduling, multiple issue, speculative execution, and branch prediction. Limits on ILP and software approaches to exploit more ILP. VLIW and EPIC approaches. Thread-level parallelism, multiprocessors, chip multiprocessors, and multi-threading. Cache coherence and memory consistency. Advanced memory hierarchy design, cache and memory optimizations, and memory technologies. Advanced topics in storage systems. Designing and evaluating I/O systems.

Prerequisite: None

II. Textbooks and References

1. Hennessy and Patterson. Computer Architecture: A Quantitative Approach, 4th ed., Morgan Kaufmann, 2007. ***Main Textbook***.
2. Patterson and Hennessy. Computer Organization & Design: The Hardware/Software Interface, 3rd ed., Morgan Kaufmann, 2005.
3. D. Culler and J.P. Singh with A. Gupta. Parallel Computer Architecture: A Hardware/Software Approach, Morgan Kaufmann, 1998.
4. J. Hayes. Computer Architecture and Organization, 3rd ed., McGraw-Hill, 1998.
5. Readings in Computer Architecture, Mark Hill (Editor), Norman Jouppi (Editor), Gurindar Sohi (Editor), Morgan Kaufmann Publishing Co., Menlo Park, CA. 1999.
6. Trace Cache: A Low Latency Approach to High Bandwidth Instruction Fetching by E. Rotenberg, S. Bennett, and J.E. Smith, Proceedings of the 29th Annual International Symposium on Microarchitecture, November 1996. First paper on trace caches.
7. Combining Branch Predictors, S. McFarling, WRL Technical Note TN-36, June 1993. Proposes the gshare branch predictor, covers a few others. See also the paper by Yeh and Patt (below).
8. Alternative Implementations of Two-Level Adaptive Branch Prediction by T.-Y. Yeh and Y. N. Patt. Proceedings of the 19th Annual International Symposium on Computer Architecture, June 1992, pp. 124-134. The classic reference on two-level branch prediction.
9. Checkpoint processing and recovery: Towards scalable large instruction window processors. By H. Akkary, R. Rajwar, and S. T. Srinivasan. In MICRO 36, December 2003. Reordering without the reorder buffer.
10. Implementation of precise interrupts in pipelined processors by J. E. Smith and A. R. Pleszkun. Proceedings of the 12th Annual International Symposium on Computer Architecture, June 1985, pp. 36-44. The original paper on reorder buffers and their alternatives.
11. The Mips R10000 superscalar microprocessor by K. C. Yeager, IEEE Micro, April 1996. One of the first out-of-order microprocessors. Uses a merged physical register file (unlike the P6).
12. The Alpha 21264 microprocessor by R. E. Kessler, IEEE Micro, Mar/Apr 1999. Another out-of-order microprocessor that also uses a merged physical register file. The 21264 was easily the fastest processor available when it came out. The "dual cluster" design that uses two copies of the register file to reduce the complexity and latency of the bypass network is particularly interesting. This paper also has a substantial discussion of the 21264 tournament branch predictor that's also described in the textbook.
13. The Microarchitecture of the Pentium® 4 Processor by Glenn Hinton et al. Intel Technology Journal, Vol. 5 Issue 1 (February 2001). Description of the Pentium 4 microarchitecture by the chief designers, includes some comparisons with P6 and some justification of the deep pipeline/high frequency design goal.

III. Evaluation of Outcomes

1. Research Report and Presentation	30%
2. Midterm Exam	30%
3. Simulation Project and Final Exam	20%+20%

IV. Class Policies

- Attendance is required
- All submitted work must be yours
- Cheating will not be tolerated

V. Course Outline

- Introduction
- Review of Advanced Processor Designs
- Instruction-Level Parallelism and Its Exploitation

Midterm Exam

- Limits of Instruction-Level Parallelism
- Multiprocessors and Thread-Level Parallelism
- Memory Hierarchy Design
- Storage Systems

Final Exam

VI. Special Dates

- Sun 5 Feb 2012 Classes Begin
- Sun 4 Mar 2012 Research proposal is due
- Sun 11 Mar 2012 Presentations of the research proposals
- Sun 25 Mar 2012 Midterm Exam (3:30-5:00)
- Sun 1 Apr 2012 Research report is due and start of presentations
- Sun 15 Apr 2012 Simulation project proposal is due
- Sun 22 Apr 2012 Presentations of the simulation project proposals
- Tue 15 May 2012 Simulation project report is due and start of simulation project demonstrations
- Sun 20 May 2012 Last Lecture
- Sun 27 May 2012 Final Exam (3:30-5:00)

VII. Sections and Instructors

Sec	Meeting Time	Room	Instructor	Office Hours	E-mail, Homepage
1	Sun, Tue 3:30-5:00	CPE 001	Dr. Gheith Abandah	Sun 12-1 Tue 9-10 Wed 10-11	abandah@ju.edu.jo, http://www.abandah.com/gheith