0907731 Advanced Computer Architecture (Spring 2012)
Midterm Exam Solution

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Instructions: Time **75** min. Closed books & notes. No calculators or mobile phones. Show your work clearly and limit your answer to the space provided. Every question has 6 points.

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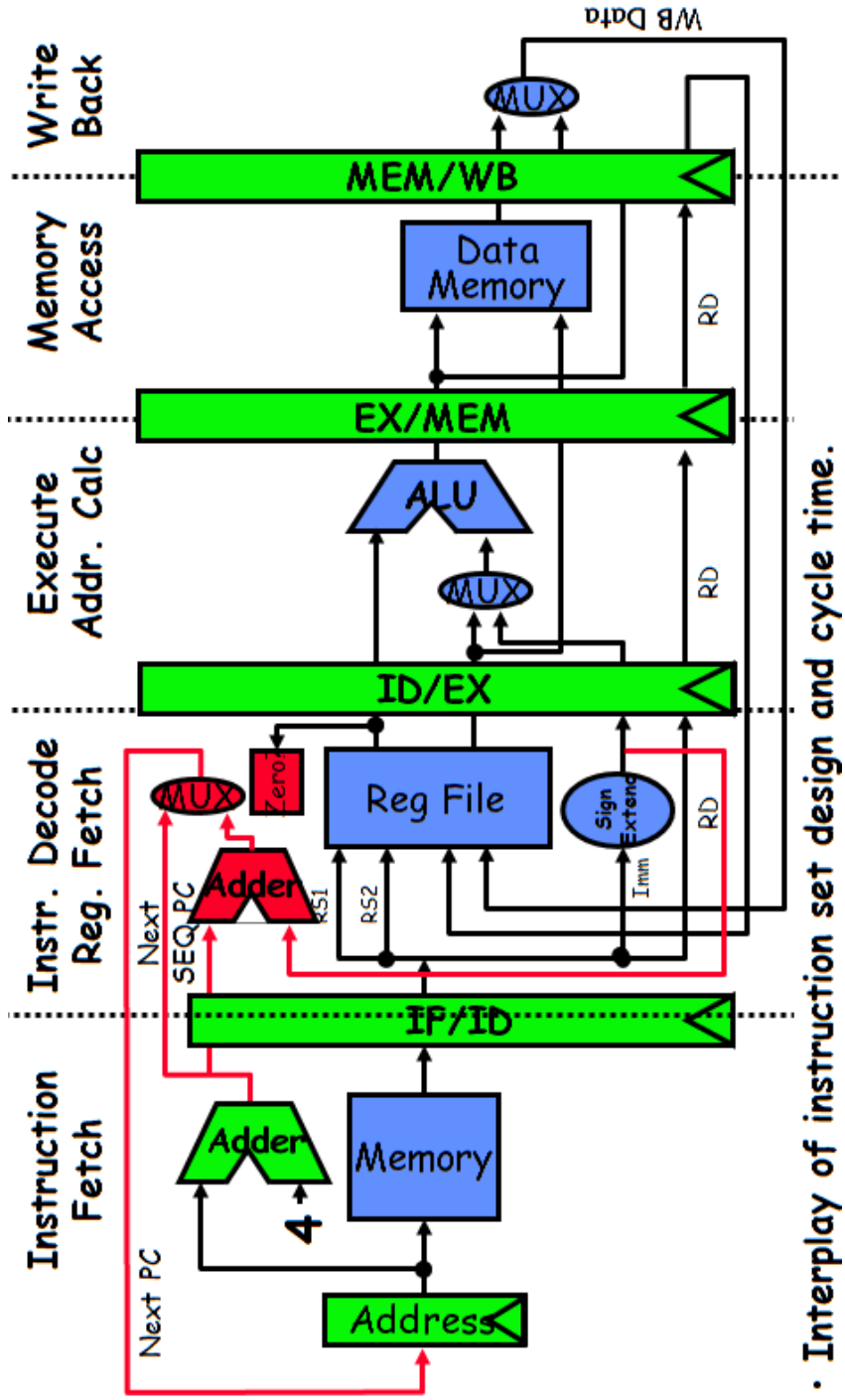
Q1. Draw a 5-stage MIPS pipeline that resolves branches in the decode stage. You need to draw the main components and busses. There is no need to draw the control signals or the forwarding paths.



Q2. Briefly describe the effect of technological advancement and Moore's law on latency and bandwidth of memory chips.

The technological advancement enables manufacturing integrated circuits with smaller transistors. The smaller transistors are faster which reduces the latency of memory chips and increases their bandwidth. Furthermore, with more transistors, the designers incorporate additional features to increase bandwidth such as wider memories and burst mode transfers. As a result the bandwidth improves faster than the latency.

Q3. Write the CPU time equation and briefly specify how its three factors are affected by instruction set and processor organization design alternatives.

CPU Time = Instruction Count (IC) * Clocks Per Instr. (CPI) * Clock Period (T)

The instruction set architecture affects:

1) **IC: more powerful set enables writing shorter programs.**
2) **CPI: simpler instruction sets allow developing processors with smaller CPI.**

The processor organization affects:

1) **CPI: superscalar designs using caches give smaller CPI.**
2) **T: pipelining allows smaller T.**

Q4. Unroll the following loop twice and schedule it, then find how many cycles are needed to execute one iteration of the unrolled loop. Assume that you have the five-stage pipeline with multi-cycle operations, FP operations take 2 cycles, branch instructions are resolved in the Decode stage, and the processor can write one integer result and one FP result in the Write Back stage every cycle.

```
Loop: l.d       F0, 0(R1)    F D E M W
      l.d       F4, 0(R2)      F D E M W
      mul.d     F0, F0, F4       F D D E E M W                    STALL
      add.d     F2, F2, F0         F F D D E E M W                STALL
      s.d       F2, 0(R3)              F F D E M W
      daddi     R3, R3, #-8                F D E M W
      daddi     R2, R2, #-8                  F D E M W
      daddi     R1, R1, #-8                    F D E W M
      bnez      R1, Loop                         F D D E M W      STALL
```

```
                          1 2 3 4 5 6 7 8 9 0 1 2 3 4 5 6 7 8
Loop: l.d       F0, 0(R1)    F D E M W
      l.d       F4, 0(R2)      F D E M W
      l.d       F6, -8(R1)       F D E M W
      l.d       F8, -8(R2)         F D E M W
      mul.d     F0, F0, F4           F D E E M W
      mul.d     F6, F6, F8             F D E E M W
      add.d     F2, F2, F0               F D E E M W
      s.d       F2, 0(R3)                  F D E M W
      add.d     F2, F2, F6                   F D E E M W
      s.d       F2, -8(R3)                     F D E M W
      daddi     R3, R3, #-16                     F D E M W
      daddi     R1, R1, #-16                       F D E W M
      daddi     R2, R2, #-16                         F D E M W
      bnez      R1, Loop                               F D E M W
```

Need 14+4 cycles to execute one iteration of the unrolled loop.

Q5. Assume that the following eight instructions are executed by a speculative superscalar processor of degree 3. This processor uses reservation stations and 48-entry reorder buffer. The integer latency is 1 cycle, the memory latency is 2 cycles, and floating-point latency is 3 cycles. The processor has one address calculation unit, one memory access unit, one integer ALU unit, one floating-point unit, and one branch unit. The processor has 5 reservation stations for each functional unit. Using pipeline diagram in the space below, find the number of cycles needed to fetch and commit these instructions.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
`lw R1, 0(R2)`	**F**	**I**	**A**	**M**	**W**	**C**											
`lw F0, 0(R1)`	**F**	**I**				**A**	**M**	**W**	**C**								
`add.d F4, F2, F0`	**F**	**I**							**E**	**E**	**E**	**W**	**C**				
`sw F4, 0(R1)`		**F**	**I**				**A**						**C**				
`lw R1, 8(R2)`		**F**	**I**	**A**	**M**	**W**							**C**				
`lw F0, 0(R1)`		**F**	**I**					**A**	**M**	**W**				**C**			
`sub.d F4, F0, F6`			**F**	**I**							**E**	**E**	**E**	**W**	**C**		
`sw F4, 0(R1)`			**F**	**I**					**A**						**C**		

Need 16 cycles to fetch and complete these eight instructions.

<Good Luck>