0907432 Computer Design (Spring 2012)

Quiz 3B

الاسم: الرقم التسلسلي: رقم الشعبة: 1

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Instructions: Time **10** minutes. Closed books and notes. No calculators. Please answer all problems in the space provided. **No questions are allowed**.

<Good Luck>

Q1. Specify the sequence of events that occurs when a processor accesses a memory location not allocated in the physical memory, i.e., there is a page fault. Assume that the processor has a TLB and the relevant page table entry points to the disk location where the requested page is stored.

- **The processor accesses the TLB to get the translation, but gets a TLB miss.**
- **The page table is accessed and a page fault exception is raised.**
- **The operating system assigns a physical page for the required virtual page and loads it from the disk.**
- **The page table is updated and the faulted instruction is restarted.**
- **The processor gets another TLB miss but the translation is copied from the page table to the TLB and the memory access is satisfied from the physical page.**

<1 mark for each of the above points>

Q2. Specify the sequence of events that occurs in a bus-based invalidating cache coherence protocol when Processor B executes a store instruction to a memory block that is dirty in the cache of Processor A.

- **Processor B gets cache miss.**
- **Processor B issues write miss request on the bus.**
- **Processor A writes back the requested block on the bus and invalidates its copy.**
- **The memory updates its contents from the data of Processor A.**
- **Processor B copies the requested block in its cache and the store instruction completes.**

<1 mark for each of the above points>