0907333 Embedded Systems (Fall 2011)

Quiz 3

الاسم: رقم التسجيل: رقم الشعبة: 3

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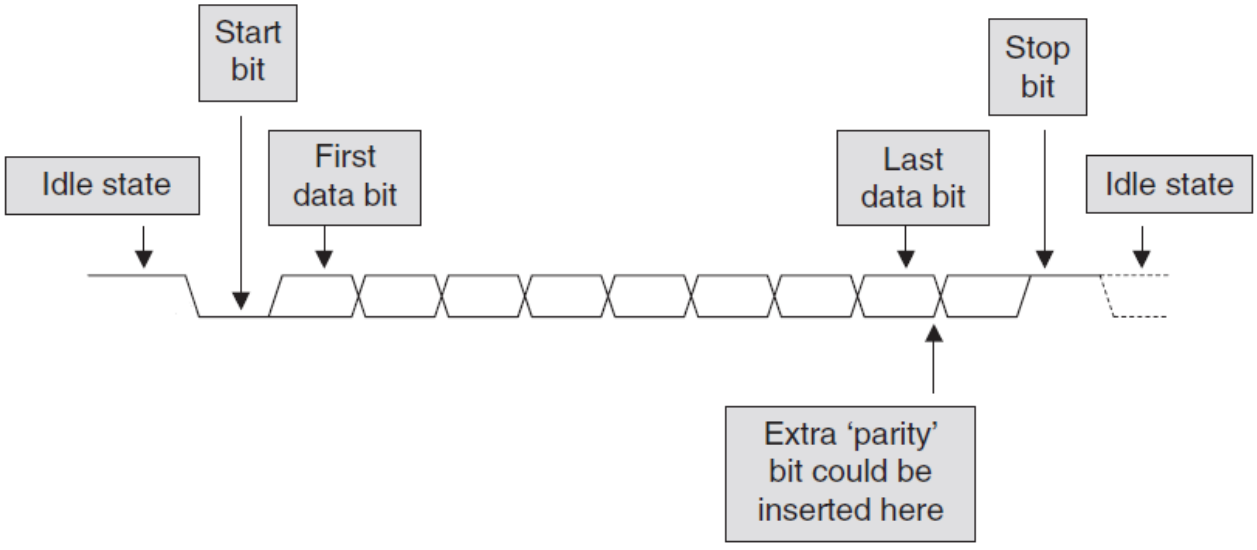
Instructions: Time **10** minutes. Closed books and notes. No calculators. Please answer all problems in the space provided. **No questions are allowed**.

<Good Luck>

Q1. Describe the common asynchronous serial data format.

The ark is out of 5.



Q2. Describe how the receiver synchronizes with the asynchronous data signal.

The mark is out of 5.

The receiver runs an internal clock whose frequency is an exact multiple of the anticipated bit rate. Usually, the receiver monitors the state of the incoming data on the serial receive line. When a Start bit is detected, a counter begins to count clock cycles until the midpoint of the anticipated Start bit is reached. It tests the state of the incoming data line again, to confirm a Start bit is present. If the Start bit is confirmed as present, the clock counter counts further cycles, to the middle of the first data bit. At this point, it clocks that bit into the main receive shift register. In this manner it continues to clock in bits, waiting each time for a bit width before clocking in the next.