University of Jordan
Computer Engineering Department
CPE702: Computer Performance Evaluation

Assignment 2
Barrel Shifter

Objective:
The objective of this experiment is to design a barrel shifter and to test the design by writing a Verilog simulation program and running it on VeriloggerPro.

Experiment:
Design an 8-bit barrel shifter that has the following control signals:

sa0, sa1, sa2	Shift amount
A	0 perform logical shift 1 perform arithmetic shift
L	0 right shift 1 left shift

The shifter should be built using basic logic gates available in the library Lib431.v.

The shifter module should be declared as follows:

```
module BarrelShifter(I, sa, A, L, O);
     input [7:0] I;
     input [2:0] sa;
     input A, L;
     output [7:0] O;
     ……..
endmodule
```

Write both the shifter module and a test module that tests the operation of this shifter. In the test module, you should test the shifter using the following input:

I	**sa**	**A**	**L**
10100101	00	0	0
10100101	01	0	0
10100101	10	0	1
10100101	11	1	0

Report:
The student should submit the schematics of the shifter, source code of the shifter module, the source code of the test module, and the output log file showing the above inputs and corresponding output. The log file must have your name printed through a $display() command.