University of Jordan
Computer Engineering Department
CPE702
Computer Performance Evaluation

Assignment 1
SR Latch Test Experiment

Objective:
The objective of this experiment is to introduce the student to the environment of the Verilog simulator, and write a simple program to simulate the operation of the SR Latch.

The VeriLogger Pro Environment:
When you start the VeriLogger Pro program, you will notice that there are four windows. The upper left is the project window; in this window you select the HDL source files to be simulated. The upper right window enables the programmer to add a free parameter. The lower left window is the place where you will see the timing diagram that shows the waveforms of the signals monitored throughout the simulation. The lower right window is the place where the contents of the log file can be seen, and the errors of compilation are displayed.

How to write a program that describes the operation of the SR-Latch? Perform the following steps:

1. Open a new project file by selecting "New HDL Project" from the Project menu. Name the project "SRLatch_Test.hpj". The name is given when you select "Save HDL Project As…" from the Project menu.
2. Open a new source file by selecting "New HDL File" from the Editor menu. A new window should appear in which you should copy the following Verilog code.

```
module main;
  reg S, R;         //declaring S and R as registers
  wire Q, Qb;       //declaring Q and Qb as wires

   SRLatch latch1(Q,Qb,S,R);  //Creating an instance of the module SRLatch

  initial begin: stop_at          //This initial begin statement selects
    #250; $stop;                  // an appropriate simulation period
  end                             //We choose it here to be 250 delay units

  initial begin: Init
    S=0; R=0;                        //Initially set S and R to zero

     // The $display statement prints the sentence between quotations in the
     // log file. It operates in the same way the printf function does
     // in the C language.
     $display(" **** Enter Your Name Here **** ");
     $display("Time      S       R       Q        Qb");

     // The monitor statement prints the values of the different
     // parameters whenever a change in the value of one of
     // them or more occurs.
     $monitor("%0d       %b        %b       %b          %b", $time, S, R, Q, Qb);
```

```
  end

  always begin: Sstate   // We use this always begin construct to
    #10 S=0;             // continuously vary the values of the input
    #10 S=1;             // registers S and R, in order to have
  end                    // a simulation whose output continuously changes.

  always begin: Rstate
    #20 R=0;
    #20 R=1;
  end
endmodule
```

3. Save this new HDL file as "Main.v" by selecting "Save HDL File As…" from the Editor menu.
4. Add Main.v you your HDL project by selecting the project window, right click in the workspace of this window, and select "Add HDL File(s)…".
5. Similar to Steps 2 through 4, add to your project a new file named SRLatch.v that contains following code.

```
// This module describes the SR Latch structurally
module SRLatch(Q,Qb,S,R);
  input S,R;
  output Q,Qb;

   NOR nor1(Qb,S,Q);
   NOR nor2(Q,R,Qb);

endmodule
```

6. Repeat these steps to add another file named Lib.v that contains the following code.

```
// This module describes the NOR Gate behaviorally
module NOR (out, in1, in2);
   input in1, in2;
   output out;

   assign #1 out =  ~(in1 | in2);
endmodule
```

7. After you have added the required files start the program simulation by clicking on the green arrow in the center of the Tool bar. The results should appear in the log file and the waveforms should appear in the timing diagram.
8. Print out the timing diagram by selecting "Print Diagram…" from the File menu.
9. Print out the log file by selecting "Print Report Tab…" from the Report menu.
10. The Timing Diagram and the Log File should be submitted.