COURSE SYLLABUS
Spring 2011

1. **Department, Number and Course Title**

Department:	Computer Engineering
Course Number:	ECE 22446
Course Title:	Microcomputer System Design

2. **Design:** Required Course

3. **Catalog Description**

Microprocessor architecture and organization, Bus architectures, types and buffering techniques, Memory and I/O subsystems, organization, timing and interfacing, Peripheral controllers and programming. Practice of the design of a microprocessor system design.

4. **Prerequisite(s)**

Digital Logic Design and Assembly Language

5. **Textbook(s) and/or other Required Material**

Barry B. Brey, The Intel Microprocessors: 8086/8088, 80186/80188, 80286, 80386, 80486, Pentium, Pentium Pro Processor, Pentium II, Pentium III, Pentium 4, and Core2 with 64-bit Extensions: Architecture, Programming, and Interfacing, 8th ed., Prentice-Hall, 2008.

1. James Antonakos, An Introduction to the Intel Family of Microprocessors, Prentice-Hall, 3ed Edition, 1999.
2. Walter Triebel and Avtar Singh, The 8088 and 8086 Microprocessors: Programming, Interfacing, Software, Hardware, and Applications, 4th ed., Prentice-Hall, 2002.
3. Intel 80x86 hardware reference manuals, Intel.

6. **Course Objectives**

- learn how the hardware and software components of a microprocessor-based system work together to implement system-level features;
- learn both hardware and software aspects of integrating digital devices (such as memory and I/O interfaces) into microprocessor-based systems;
- learn the operating principles of, and gain hands-on experience with, common microprocessor peripherals such as UARTs, timers, and analog-to-digital and digital-to-analog converters;
- get practical experience in applied digital logic design and assembly-language programming; and
- be exposed to the tools and techniques used by practicing engineers to design, implement, and debug microprocessor-based systems (during the Lab).

7. **Topics Covered**

- 80x86 Processor Architecture: Introduction, Processor Model, Programmer's model, Designer's Model: 8086 hardware details, Clock generator 8284A, Bus buffering and latching, Processor Read & Write bus cycles, Ready and wait state generation, Minimum versus Maximum mode operation.
- Memory Interfacing: 80x86 processor-Memory interfacing, Address decoding techniques, Memory Devices – ROM, EPROM, SRAM, FLASH, DRAM devices, Memory internal organization, Memory read and write timing diagrams**,** DRAM Controller
- Basic I/O Interfacing: Parallel I/O, Programmed I/O, I/O port address decoding, The 8255A Programmable Peripheral Interface (PPI), programming 8255, Operation modes, Interface examples – Keyboard matrix, LCD/7-Segment Display, Printer, stepper motor, A/D and D/A converter.
- Timer Interfacing: The 8254 Programmable Interval Timer (PIT), Timing applications.
- Serial I/O Interface**:** Asynchronous communication, Physical communication standard-EIA RS232, Programmable Communication Interface - UART 8251, Interfacing serial I/O devices- mouse, modem, PC Keyboard.
- Interrupts: Interrupt driven I/O, Software & Hardware interrupts, Interrupt vectors and vector table, Interrupt processing, The 8259A Programmable Interrupt Controller (PIC)- cascading of 8259s, programming 8259, Interrupt examples – Printer, Real-Time Clock, PC Keyboard.
- Direct Memory Access: Basic DMA operation, DMA Controlled I/O, The 8237 DMA Controller, Disk Memory Systems- Floppy disk, Hard disk, optical disk memory systems, video displays
- Bus Interfaces: PC bus standards & interfaces – PCI, USB, Firewire, AGP

8. **Course Contribution to Meet the Professional Component**

This course is tightly integrated with a lab component which exposes the student to various aspects of microprocessor engineering including signal analysis, design & fabrication of medium-sized 80x86 microprocessor based system, manual wiring, testing, hardware troubleshooting, and conducting I/O interfacing experiments using professional processor kits.

9. **Relationship to Program Outcomes**

This course supports the following seven program outcomes out of the outcomes required by ABET Criterion 3 for accrediting computer engineering programs.

Outcome1: Ability to apply knowledge of mathematics, probability, and engineering in microprocessor based system design. [ABET Criterion 3a]

Outcome 2: Ability to design and conduct experiments related to microprocessor based system design and to analyze their outcomes. [ABET Criterion 3b]

Outcome 3: Ability to design, debug and test a small scale microprocessor system. [ABET Criterion 3c]

Outcome 4: Ability to identify, formulate, and solve engineering problems in microprocessor based system design. Ability to function as an effective team member. [ABET Criterion 3d]

Outcome 5: Ability to identify, formulate, and solve engineering problems in microprocessor based system design. [ABET Criterion 3e]

Outcome 6: Ability to use design tools for microprocessor system design, test and evaluation. [ABET Criterion 3k]

Outcome 7: Ability to engage in self-learning. [ABET Criterion 3i]

Course Learning Outcomes	**Outcome Indicators and Details**	**Assessment Methods and Metrics**
O1. Ability to apply knowledge of mathematics, probability and engineering in microprocessor based system design	➢ Analysis of bus Fan-in and Fan-out requirements, analysis of bus and processor timing, performance evaluation, ➢ CPU execution time ➢ memory access time and bandwidth ➢ wait state computation ➢ computation of timing delays ➢ I/O performance such as interrupt latency and DMA speed	• Assignments • Exams
O2. Ability to design and conduct experiments related to microprocessor based system design and to analyze their outcomes.	➢ Design & conduct experiments on clock generation, power-on-reset generation, ready synchronization, address decoding, memory interfacing and I/O interfacing	• Lab work
O3. Ability to design, debug and test a small scale microprocessor based system	➢ Design of Clock generation, Reset generation & synchronization, Wait state computation & generation, Ready synchronization, ➢ Address bus latching, data bus buffering, Design of Memory Map, Memory Address decoder, Memory Read and write logic ➢ Interfacing of RAM and EPROM memories. to processor(appropriate selection and connection of address bus, data bus, read/write control and chip select) Modes of I/O data transfer – Programmed or Polled I/O, Interrupt driven I/O, DMA ➢ Design of I/O Map, I/O address decoder and I/O Read and Write logic Interfacing of Parallel & Serial I/O devices to processor using peripheral chips 8255 PPI, 8254 PIT. - appropriate selection and connection of address bus, data bus, read/write control, chip select between processor and peripheral chips - data, control and status signal interconnections between peripheral chips and I/O devices - Programming of Peripheral interfacing chips ➢ debug and test the design as well as to develop small test program to test the design correctness and timing versus some requirements. ➢ Revise the design appropriately	• Assignments • Exams • Lab work

	➢ Report and document the design.	
O4. Ability to function as an effective team member	➢ Working in a team to design, assemble and test a small microprocessor based system prototype	• Lab work
O5. Ability to identify, formulate, and solve engineering problems in microprocessor based system design	➢ Identify, formulate and solve engineering problems in the microprocessor based system design considering the following : - Enhancements in the processor internal architecture, processor address & data bus width - Latest trends and developments in Memory Technology (SRAM, DRAM, SDRAM, RDRAM, DDR/DDR2) - Recent developments in I/O interfacing standards and I/O devices	• Assignments • Exams • Lab work
O6. Ability to use design tools for microprocessor system design, test and evaluation..	➢ Use of tools for debugging, develop techniques for testing, and use of trace analysis and timing for evaluation ➢ Use of Logic analyzers, oscilloscopes, logic probes, multimeters ➢	• Lab work
O7. Ability to engage in self-learning	➢ Demonstrates reading and writing skills ➢ Identifying, retrieving, and organizing information ➢ Following a learning plan ➢ Demonstrate critical thinking skills such as applying the facts, formulae, theories, etc. to everyday situations.	• Assignments • Exams