Homework 2

Due on the Second Exam day on Mon 27/12/2010. Must be handwritten.

Q1. Assume that the following code sequence is executed by a single-issue speculative processor. This processor uses reservation stations and reorder buffer. The integer latency is 1 cycle and the load latency is 2 cycles. The processor has one address calculation unit, one memory access unit, one integer ALU unit, and one branch unit. Assume that the processor predicts that the branch instruction is not taken and the branch is actually taken. Using a pipeline diagram in the space below, illustrate the execution of these instructions in this processor pipeline.

```
                                1  2  3  4  5  6  7  8  9  0  1  2  3  4  5
    lw          R2, 0(R1)
    beq         R2, ZERO, Skip
    lw          R3, 0(R2)
Skip:
    add         R4, R3, R3
```

Q2. Use register renaming to rewrite the following code segment to eliminate WAW and WAR dependencies.

```
    lw          R2, 0(R1)
    beq         R2, R3, Skip
    add         R3, R2, R2
Skip:
    add         R2, R3, R3
```

Q3. The Opteron X4 pipeline has the bottlenecks listed below. Suggest design techniques to reduce these bottlenecks.

(a) Complex instructions with long dependencies
(b) Branch mispredictions
(c) Memory access delays

Q4. Draw the Opteron X4 micro-architecture.

Q5. For a direct-mapped cache design with 32-bit address, the following bits of the address are used to access the cache.

Tag	Index	Offset
31-6	5-4	3-0

(a) What is the cache line size (in words)?
(b) How many lines does the cache have?
(c) What is the ratio between total bits required for such a cache implementation over the data storage bits?
(d) Starting from power on, fill the following table for the hexadecimal byte-addressed cache references shown.

Address	Block Address	Cache Index	Hit or Miss
00000024			
0000002C			
000000A0			
00000004			
0000002C			
00000059			
0000006C			
000000A4			

(e) How many blocks are replaced? _____
(f) What is the hit ratio? _____

Q6. Given a 256 Kbyte cache, a 4 Gbytes memory address space, and a cache block size of 64 bytes,

(a) For a direct mapped cache, how many bits are allocated to the tag?
(b) What extra status bit is found in a write-back cache and not needed in a write-through cache?

Q7. Given a memory module made of Synchronous DRAM chips that run on a frequency of 400 MHz. If the module has 32-bit data bus and 50-ns access latency for the first word in the page mode operation, what is the time needed to access a four-word block?

Q8. Design a 32-byte direct mapped cache that has 8-byte blocks. Assume that the processor has 32-bit address and 32-bit data busses. Your design should show the cache memory (specify number of blocks), the hit circuit, and the multiplexer.

Q9. Given the following memory hierarchy specifications, what is the average memory access time in cycles?

L1 Cache: Hit time = 1 cycle, miss rate = 5%

L2 Cache: Hit time = 10 cycles, miss rate = 1%

Main Memory: Access time = 100 cycles