22541 Computer Architecture (Fall 2010)
Second Exam Solution

الاسم: رقم التسجيل: رقم الشعبة: 1

==========

Instructions: Time **60** min. Closed books & notes. No calculators or mobile phones. No questions are allowed. Show your work clearly. Every problem is for 5 marks.

==========

Q1. Assume that the following code sequence is executed by a single-issue speculative processor. This processor uses reservation stations and reorder buffer. The integer latency is 1 cycle and the load latency is 2 cycles (one cycle for address calculation and one cycle for memory access). The processor has one address calculation unit, one memory access unit, one integer ALU unit, and one branch unit. Assume that the processor predicts that the branch instruction is not taken and the branch is actually taken. Using a pipeline diagram in the space below, illustrate the execution of these instructions in this processor pipeline.

```
                                1  2  3  4  5  6  7  8  9  0  1  2  3  4  5
    lw        R2, 0(R1)         F  I  A  M  W  C
    beq       R2, ZERO, Skip       F  I  -  -  E  W  C
    add       R2, R2, R5              F  I  -  E  -  n
    sw        R3, 0(R2)                  F  I  A  -  n
Skip:
    add       R4, R3, R3                    F  I  E  n  F  I  E  W  C
```

n: flushing the instruction to null.

Q2. Use register renaming to rewrite the following code segment to eliminate WAW and WAR dependencies.

```
    lw        R2, 0(R1)
    add       R3, R2, R2
    sw        R3, 0(R1)
    lw        R2, 4(R1)       -> lw     R4, 4(R1)
    add       R3, R2, R2      -> add    R5, R4, R4
    sw        R3, 4(R1)       -> sw     R5, 4(R1)
```

Q3. For a two-way associative cache design with 32-bit address, the following bits of the address are used to access the cache. Assume that the cache uses the LRU replacement policy.

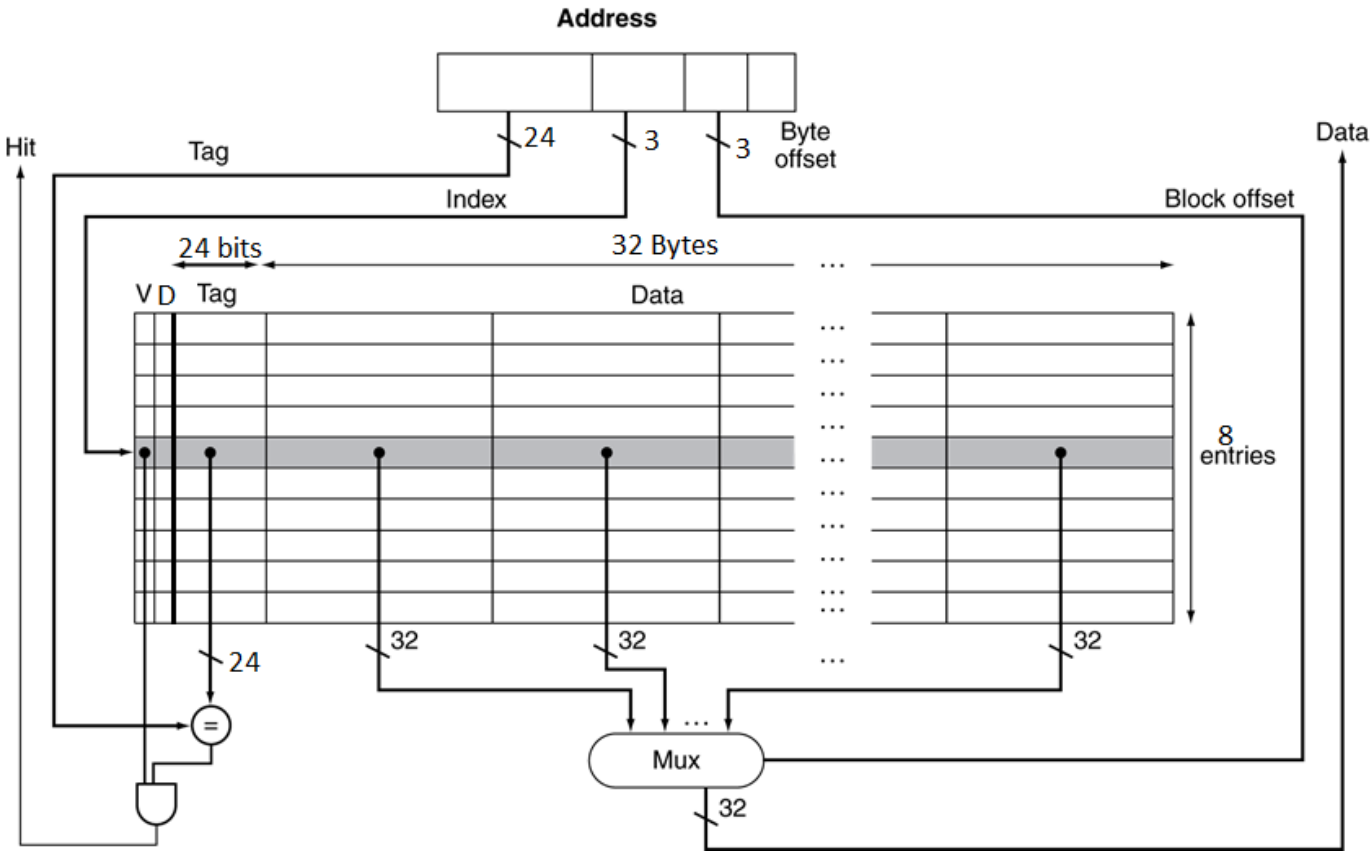
Tag	Index	Offset
31-6	5-4	3-0

(a) How many lines does the cache have? ___$2 * 2^2 = 8$____

(b) Starting from power on, fill the following table for the hexadecimal byte-addressed cache references shown.

Address	Block Address	Cache Index	Hit or Miss
00000024	2	2	M
0000002C	2	2	H
000000A0	A	2	M
00000004	0	0	M
0000002C	2	2	H
00000008	0	0	H
0000006C	6	2	M
000000A4	A	2	M

Q4. Design a 256-byte direct mapped cache that has 32-byte blocks. Assume that the processor has 32-bit address and 32-bit data busses and uses the write-back policy. Your design should show the cache memory (specify number of blocks), the hit circuit, and the multiplexer.



5. Given the following memory hierarchy specifications, what is the average memory access time in cycles?

L1 Cache: Hit time = 1 cycle, miss rate = 5%

L2 Cache: Hit time = 10 cycles, miss rate = 1%

L3 Cache: Hit time = 30 cycles, miss rate = 0.5%

Main Memory: Access time = 400 cycles

$AMAT_{L3}$ = 30 + 0.005 * 400 = 30 + 2 = 32 Cycles

$AMAT_{L2}$ = 10 + 0.01 * 32 = 10 + 0.32 = 10.32 Cycles

$AMAT_{L1}$ = 1 + 0.05 * 10.32 = 1 + 0.516 = 1.516 Cycles

<Good Luck>