University of Jordan
Computer Engineering Department
CPE439: Computer Design Lab

Experiment 7: Data Memory Module – Part II

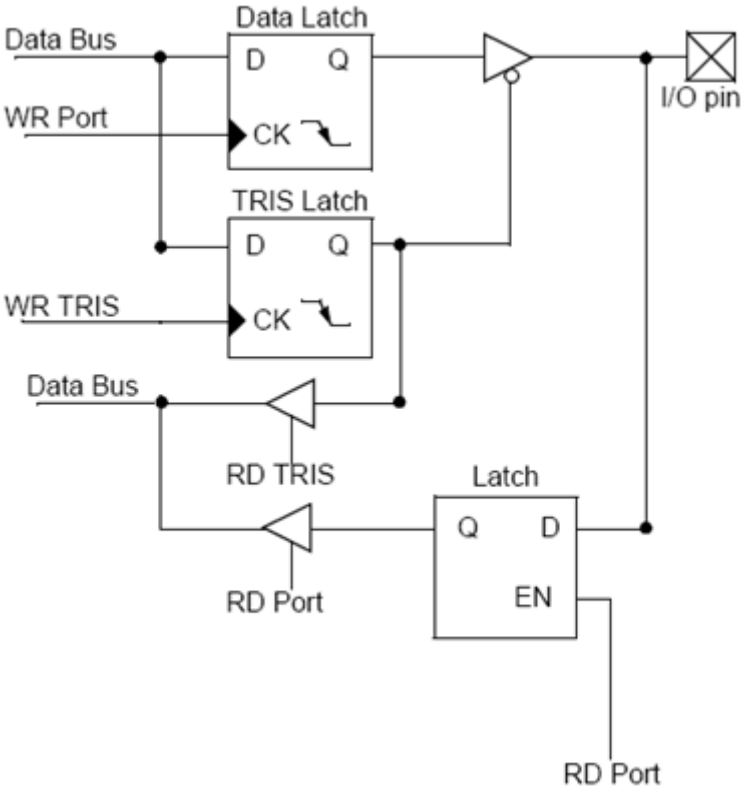
It is required to complete constructing and testing the Verilog module for a data memory suitable for incorporation in your PIC16F84A design. You need to complete the circuits of the special function registers: STATUS, PORTA, PORTB, TRISA, and TRISB.

Status Register

The Status register must be implemented using individual flip-flops so that each bit of the three status bits (C, DC, and Z) could be updated individually. This is in addition to the ability to read and write this register as an 8-bit register similar to the other data memory locations.

Parallel Input/Output

The following circuit shows how to build a configurable input/output port. Duplicate this circuit (with other needed logic) to implement PIC's Port A and Port B.



Report

Your report should include detailed design, Verilog code for all modules including your test modules, and timing diagram that demonstrates the correct operation of your design.