

Problems with Pipelining

- **Exception:** An unusual event happens to an instruction during its execution
 - Examples: divide by zero, undefined opcode
- **Interrupt:** Hardware signal to switch the processor to a new instruction stream
 - Example: a sound card interrupts when it needs more audio output samples (an audio “click” happens if it is left waiting)
- **Problem:** It must appear that the exception or interrupt must appear between 2 instructions (I_i and I_{i+1})
 - The effect of all instructions up to and including I_i is totalling complete
 - No effect of any instruction after I_i can take place
- The interrupt (exception) handler either aborts program or restarts at instruction I_{i+1}

The diagram illustrates the MIPS processor architecture, showing the flow of instructions and the handling of exceptions. The main stages are PC (Program Counter), Inst. Mem (Instruction Memory), D (Data Memory), Decode, E (Execute), ALU (+), M (Memory), Data Mem (Data Memory), and W (Write Back). The PC stage includes a Select Handler PC input. The D stage includes a PC Address Exceptions input. The Decode stage includes an Illegal Opcode input. The E stage includes an Overflow input. The M stage includes a Data Addr Except input. The Data Mem stage includes a Kill Writeback input. The W stage includes a Cause and EPC input. The diagram also shows the flow of exceptions: PC Address Exceptions, Illegal Opcode, Overflow, Data Addr Except, and Kill Writeback. The diagram also shows the flow of instructions: PC, Inst. Mem, D, Decode, E, ALU (+), M, Data Mem, and W. The diagram also shows the flow of the PC: PC, PC D, PC E, PC M, and PC W. The diagram also shows the flow of the ALU: ALU (+). The diagram also shows the flow of the Data Mem: Data Mem. The diagram also shows the flow of the W: W. The diagram also shows the flow of the Cause: Cause. The diagram also shows the flow of the EPC: EPC. The diagram also shows the flow of the Kill F Stage: Kill F Stage. The diagram also shows the flow of the Kill D Stage: Kill D Stage. The diagram also shows the flow of the Kill E Stage: Kill E Stage. The diagram also shows the flow of the Asynchronous Interrupts: Asynchronous Interrupts. The diagram also shows the flow of the Commit Point: Commit Point.

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