Computer Design (0907432)
Homework 1

Submit Handwritten Solutions

1. State the six reasons why latency improvements lag bandwidth improvements.

2. Why processor manufacturers have recently shifted to building multicore processors instead of building larger and faster uni-processors?

3. A program consists of multiplication operations and other operations. The multiplication operations are sped up by a factor of 5. Using Amdahl's law, find out what should be the fraction of the execution time of the multiplication operations (f) to achieve an overall speed up of 4.

4. Calculate FIT and MTTF for a system that has 3 disks (1M hour MTTF per disk), 2 CPUs (2M hour MTTF per CPU), and 4 memory modules (0.5M hour MTTF per module).

5. For the data shown in the following table, summarize the relative performance of Machine A using one number.

Benchmark	**Machine A Execution Time**	**Reference Machine Execution Time**
1	100 sec	500 sec
2	75 sec	400 sec
3	200 sec	450 sec
4	150 sec	350 sec

6. Write code sequences to implement D=A*(B-C+A); on the four ISA classes.

7. Show how to implement the addressing modes in Figure B.6 using register, immediate, and register indirect addressing modes.

8. Using pipeline diagrams, find how many cycles are needed to execute the following code sequence.
    a. When stalls are used to solve hazards and branch instructions are resolved in the Execute stage.
    b. When full forwarding paths are used plus stalls (when needed), one branch delay slot, and branch instructions are resolved in the Decode stage.

```
      lw    r1, 0(r2)
      lw    r3, 4(r2)
      add   r4, r1, r3
      sw    r4, 0(r2)
      beq   r4, r4, skip
      andi  r4, r4, 0
skip: sw    r4, 4(r2)
```