0907432 Computer Design (Spring 2009)
Midterm Exam

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Instructions: Time **45** min. Closed books & notes. No calculators or mobile phones. **No questions are allowed**. Show your work clearly and write your final answer in the underlined space. For multiple-choice questions, put an "x" mark for the **best** answer. Every problem is for 2.5 marks.

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Q. The most important thing that the computer designer focuses on when designing a personal computer is:

☐ Throughput ☒ **Price-Performance** ☐ Power
☐ Usability ☐ Scalability

Q. A processor takes 2 seconds to execute the floating-point operations of a program and 2 seconds to execute the rest operations. To achieve an overall speedup of 2 on this program, the execution of the floating-point operations should be enhanced by a factor of: ____∞_____

Speedup = 1 / (1-f + f/s)
f = 2 / (2 + 2) = 0.5
2 = 1 / (1-0.5 + 0.5/s)
1 + 1/s = 1
1/s = 0
s = ∞

Q. The minimum number of instructions needed by an accumulator computer to evaluate "A = B * C" is (assume that A, B, and C are variables in the memory): ___**3**____

```
ld   B
mul  C
st   A
```

Q. The instruction below uses the memory auto-increment addressing mode, which is not supported in MIPS. In the space provided to the right, implement this instruction using valid MIPS instructions.

`add r1, (r2)+`	`add r1, 0(r2)`
	`addi r2, 4`
	or
	`lw r1, 0(r2)`
	`add r1, r1, ra`
	`addi r2, r2, 4`

Q. The number of anti-dependencies in the following MIPS code sequence is: ____**2**_____

```
add     r1, r2, r3
addi    r2, r1, #1      r2 with r2 in add
sub     r3, r1, r2      r3 with r3 in add
bne     r1, r3, Skip
```

Q. A processor supports multi-cycle operations as described in the class. This processor has the standard F, D, E, M, and W stages, but the floating-point operations go through stages A1, A2, A3, and A4 instead of the E stage. Use pipeline diagrams to determine the minimum number of cycles needed to execute the following code sequence. Assume that the processor uses stalls and register flags to solve data hazards. The number of cycles is: _____**14**____ (state any assumption you make)

```
                    1 2 3 4 5 6 7 8 9 0 1 2 3 4
add.d   f0, f1, f2  F D A A A A M W
sub.d   f3, f0, f4    F D - - - - - A A A A M W
```

I assumed that the register file supports writing and reading in the same cycle (split-cycle operation).

Q. A processor uses Tomasolu's approach to execute instructions out of order. For the following code sequence, assume that the first instruction is issued to reservation station 'Mul1 and the second instruction to 'Add1'. Also assume that the first instruction has not finished.

```
mul.d       f2, f0, f8
sub.d       f4, f2, f6
```

Complete the following reservation station entry.

Reservation Station	Busy	Op	Dest.	Source Register		Source RS	
				Fj	Fk	Qj	Qk
Add1	**Yes**	**sub.d**	**f4**		**Reg[f6]**	**Mul1**	

Q. A branch history table with n=1 is better than one with n=2 in the following case:

☐ Loop executed one iteration ☐ Loop executed two iterations ☐ Loop executed 10 iterations
☐ **Conditional branch that is 10 times not taken then 10 times taken** ☐ None of the above

Q. Assume that you have an (m, n) correlating branch predictor where m=2, n=2, and k=11. The size of this predictor in Kbits is _____**16**_____

Size = $2^m * n * 2^k = 2^2 * 2 * 2^{11}$ = 16 Kbits

Q. Assume that the following code sequence is executed by a superscalar processor of degree 2. Assume that this processor uses static scheduling as the example described in the class where the processor has an integer ALU unit and FP unit. Assume that any stage takes one cycle. The number of cycles needed to execute these instructions is: ___**6**____

```
                          1 2 3 4 5 6
lw          R2, 0(R1)     F D E M W
lw          R3, 4(R1)     F D - E M W
add.d       F0, F2, F4      F D A M W
```

Q. Assume that the following code sequence is executed by a speculative processor. This processor uses reservation stations and reorder buffer. The processor has address calculation unit, memory access unit, and integer ALU unit. Each stage takes one cycle. The number of cycles needed to issue and commit these instructions is: ___**8**____

```
                          1 2 3 4 5 6 7 8
lw          R2, 0(R1)     I E M W C
lw          R3, 4(R1)       I E M W C
add         R4, R2, R3        I - - E W C
```

Q. Consider the instruction sequence shown below. In the space provided to the right, use pipeline scheduling to rewrite this sequence to get faster execution on the 5-stage MIPS pipeline described in the class.

```
lw      r1, 0(r2)
add     r1, r1, r1
add     r1, r3, r5
```

```
lw      r1, 0(r2)
add     r6, r3, r5
add     r1, r1, r1
```

<Good Luck>