Computer Design
CPE 432
Homework 1

- Solve the following problems from Chapter 1 of your textbook: **1.1, 1.4, 1.9, 1.10, and 1.14**.

- Show how to implement the addressing modes in Figure B.6 using the first three addressing modes.

- Write code sequences to implement D=(A-B)*(A-C); on the four ISA classes.

- Using pipeline diagrams, find how many cycles are needed to execute the following code sequence.
    a. When stalls are used to solve hazards and branch instructions are resolved in the Execute stage.
    b. When full forwarding paths are used plus stalls (when needed), one branch delay slot, and branch instructions are resolved in the Decode stage.

```
      lw    r1, 0(r2)
      add   r3, r1, r1
      sw    r3, 0(r2)
      beq   r4, r4, skip
      andi  r3, r3, 0
skip: sw    r3, 4(r2)
```

1.1

Chip	Die Size mm²	Defect rate per cm²	Size nm	Transistors millions
~~IBM Power5~~	389	.30	130	276
Sun Niagra	380	.75	90	279
AMD Opteron	199	.75	90	233

a) AMD Opteron Yield

$$\text{Die Yield} = \text{Wafer Yield} \times \left(1 + \frac{\text{Defects per unit area} \times \text{Die Area}}{4.0}\right)^{-4.0}$$

$$\text{Yield} = 0.75 \times \frac{199}{10 \times 10} = 0.75 \times 1.99$$

$$\text{Yield} = \left(1 + \frac{0.75 \times 199/100}{4.0}\right)^{-4.0} = (1.37)^{-4.0}$$

$$= 0.28$$

b) Sun Niagara Yield

$$\text{Yield} = \left(1 + \frac{0.75 \times 380/100}{4.0}\right)^{-4.0} = (1.71)^{-4.0}$$

$$= 0.12$$

c) Because the Niagara chip is larger
so it has large probability of defects per die

4

	Product	Perf. P	Power
Processor	Sun Niagara 8-core	1.2 GHz	72-79W peak
DRAM	Kingston 1GB	184-pin	~~48.9-66~~ 2.3W
HD	DiamondMax 16	5400 rpm	7.0W, 2.9W idle
	DiamondMax 9	7200 rpm	7.9W, 4.0W idle

a) Maximum load, P.S. efficiency = 70%

P.S. wattage = ?

1 Niagara + 2 GB memory + 2 HD

Peak Power Consumption = $79 + 2 * 2.3 + 2 * 7.9$

$= 79 + 4.6 + 15.8$

$= 99.4$

P.S wattage = $99.4 / 0.7$

$= 142$ W

b) HD 40% idle

HD Power Consumption = $0.4 * 4.0 + 0.6 * 7.9$

$= 1.6 + 4.74$

$= 6.34$ W

c) 5400 idle time = ?

Idle time = $1 - \left(0.6 * \frac{7200}{5400}\right) = 1 - 0.8$

$= 0.2$

1.9 Single Processor

(a) FIT = 100 , MTTF = ?

$$MTTF = \frac{10^9}{100} = 10^7 \text{ hours}$$

(b) MTTR = 24 hours , availability = ?

$$\text{Availability} = \frac{MTTF}{MTTF + MTTR} = \frac{10^7}{10^7 + 24} =$$

$$= 99.99976\ \%$$

1.10 1000 processors , MTTF = ?

$$FIT = 1000 * 100 = 100{,}000$$

$$MTTF = \frac{10^9}{100{,}000} = 10^4 \text{ hours}$$

1.14 Dual Processor

Application 1 needs 80% of the resources

" 2 " 20% " " "

a) 40% of App 1 is parallelizable

$$\text{Speedup} = \frac{1}{(1-f) + f/s} = \frac{1}{1-0.4 + 0.4/2}$$

$$= \frac{1}{0.6 + 0.2} = \frac{1}{0.8} = \underline{1.25}$$

b) 99% of App 2 is parallelizable

$$\text{Speedup} = \frac{1}{1-0.99 + 0.99/2} = \frac{1}{0.01 + 0.495}$$

$$= \frac{1}{0.505} = \underline{1.98}$$

c) Parallelize ~~System~~ App 1

$$\text{System Speedup} = \frac{1}{0.2 + 0.8/1.25} = \frac{1}{0.2 + 0.64}$$

$$= \frac{1}{0.84} = \underline{1.19}$$

d) Parallelize App 2

$$\text{System Speedup} = \frac{1}{0.8 + 0.2/1.98} = \frac{1}{0.8 + 0.101}$$

$$= \frac{1}{0.9} = \underline{1.11}$$

Addressing Modes

- Register indirect Add r4,(r1) ≡ Add r4, 0(r1)
- Indexed Add r3,(r1+r2) ≡ Add r1, r2
  Add r3, 0(r1)
- Direct Add r1, (100#) ≡ Add r1, 100#(r0)
- Mem indirect Add r1, @(r3) ≡ lw r3, 0(r3)
  Add r1, 0(r3)
- Auto inc Add r1, (r2)+ ≡ add r1, 0(r2)
  Addi r2, # 4
- Auto dec Add r1, -(r2) ≡ Addi r2, # -4
  add r1, 0(r2)
- Scaled Add R1, 100(R2)[R3] ≡ muli r3, #4
  add r2, r3
  add r1, 100(r2)

ISA Classes

$D = (A + B) * (A - C)$;

(a) Stack

```
push  A
push  B
sub
push  A
push  C
sub
mul
pop   D
```

(b) Accumulator

```
lw   A
sub  B
sw   T
lw   A
sub  C
mul  T
sw   D
```

(c) Register-Memory

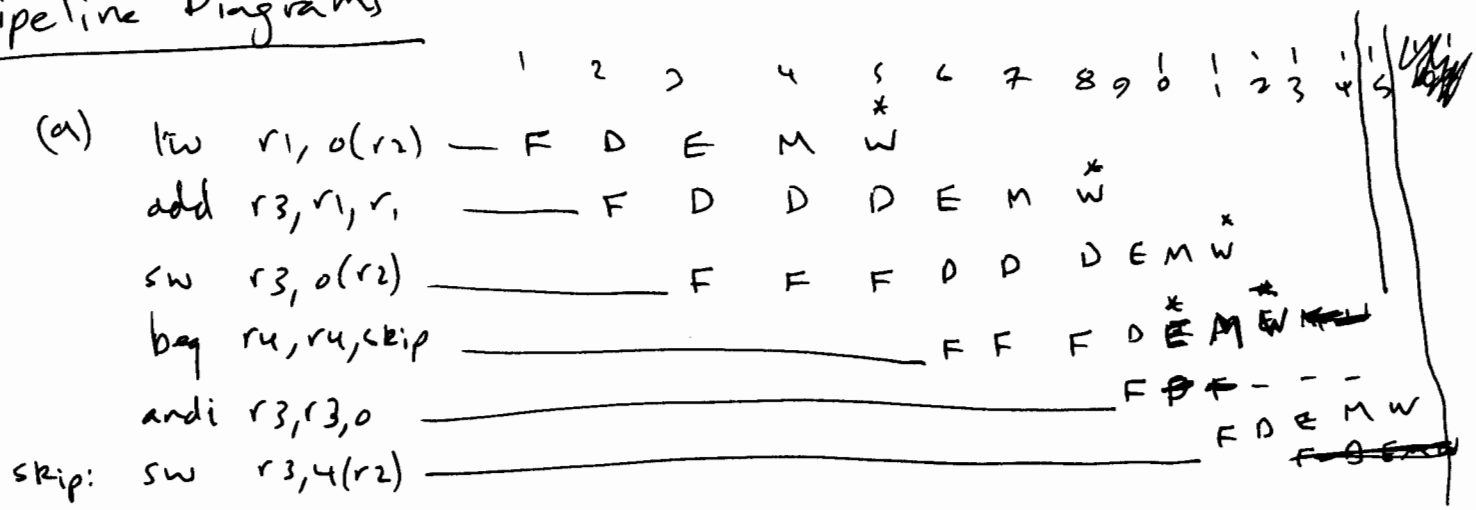
```
lw   r1, A
sub  r1, B
lw   r2, A
sub  r2, C
mul  r1, r2
sw   r1, D
```

(d) Register-Register

```
lw   r1, A
lw   r2, B
sub  r1, r2
lw   r3, A
lw   r4, C
sub  r3, r4
mul  r1, r3
sw   r1, D
```

Pipeline Diagrams

(a)



(b)