0907231 Digital Logic (Fall 2009)
Quiz 2B Solution

الاسم: رقم التسجيل: رقم الشعبة: 2

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Instructions: Time **20** minutes. Closed books and notes. No calculators. **No questions are allowed**.

Q1. *Clock*, *S* and *R* waveforms, one latch and two flip-flops are shown in the figure below. For the latch and the flip-flops, carefully sketch the output waveform, Q_i, obtained in response to the input waveforms. Assume that the propagation delay of the storage elements is negligible. Initially, all storage elements store 0.
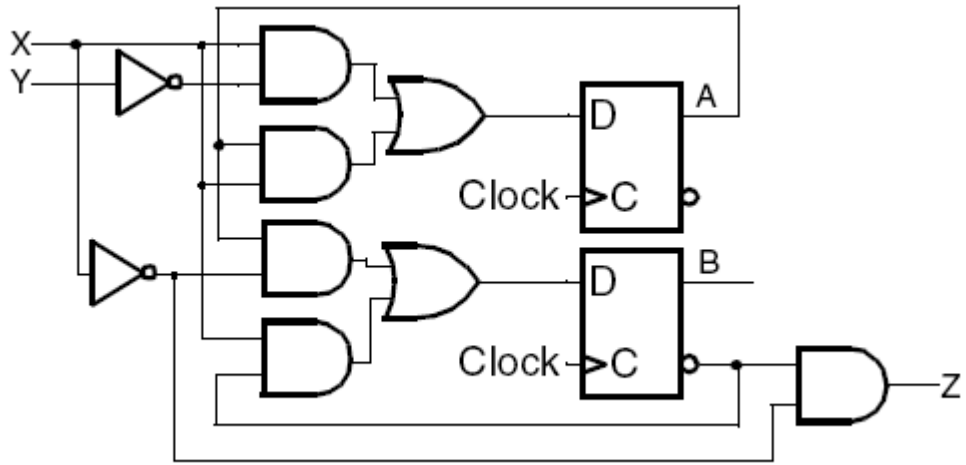
<3 marks>
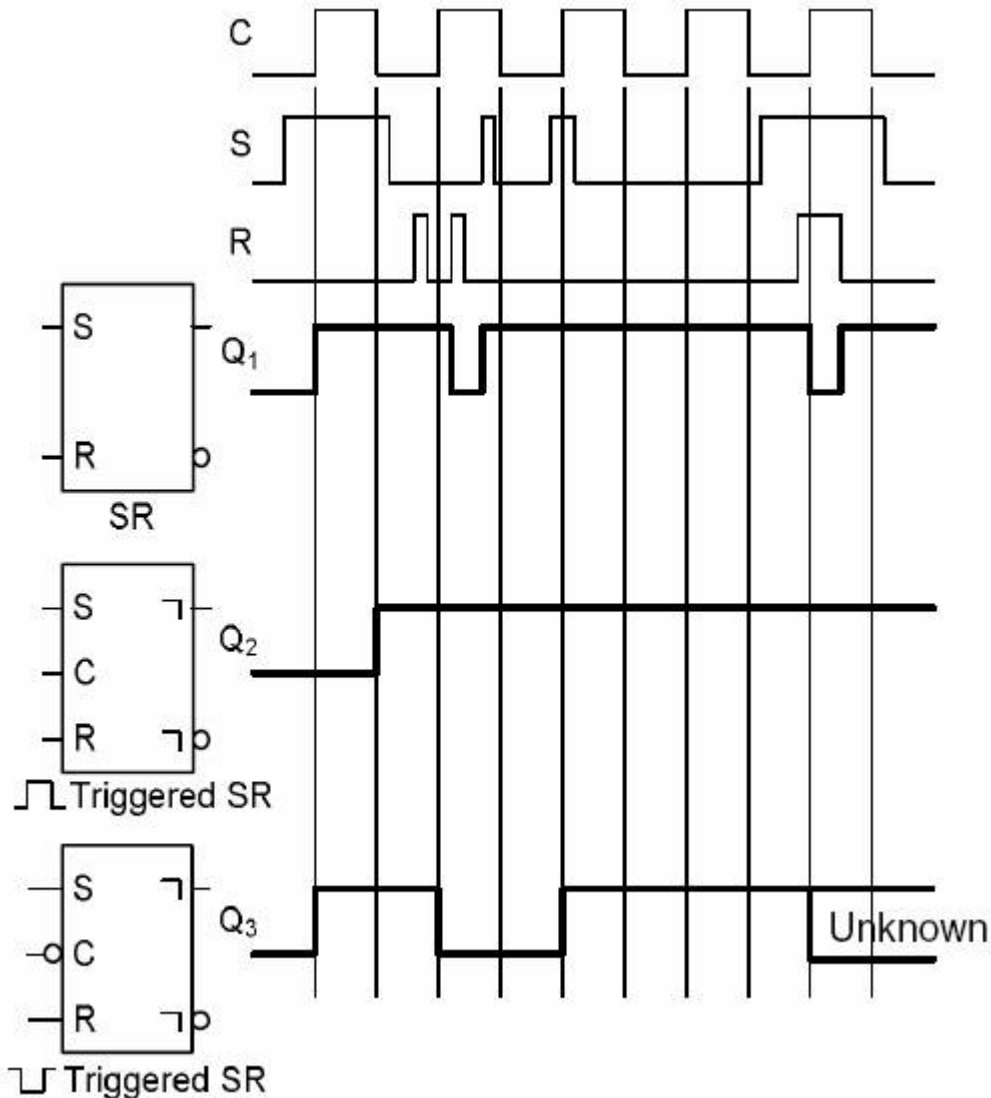
Q2. A sequential circuit with two D flip-flops *A* and *B*, two inputs *X* and *Y*, and one output *Z* is specified by the following input equations:

$$D_A = XA + X\bar{Y}, \quad D_B = X\bar{B} + \bar{X}A, \quad Z = \bar{X}\bar{B}$$

(a) Draw the logic diagram of the circuit.
(b) Derive the state table.
(c) Derive the state diagram.

<3 marks>

Present State		Inputs		Next State		Output
A	**B**	**X**	**Y**	**A**	**B**	**Z**
0	0	0	0	0	0	1
0	0	0	1	0	0	1
0	0	1	0	1	1	0
0	0	1	1	0	1	0
0	1	0	0	0	0	0
0	1	0	1	0	0	0
0	1	1	0	1	0	0
0	1	1	1	0	0	0
1	0	0	0	0	1	1
1	0	0	1	0	1	1
1	0	1	0	1	1	0
1	0	1	1	1	1	0
1	1	0	0	0	1	0
1	1	0	1	0	1	0
1	1	1	0	1	0	0
1	1	1	1	1	0	0

00/1
01/1

11/0

10/0

00/0
01/0
11/0

10/0

10/0
11/0

00/1
01/1

10/0
11/0

00/0
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00

01

10

11